Special Papers

MOS Operational Amplifier Design— A Tutorial Overview

PAUL R. GRAY, FELLOW, IEEE, AND ROBERT G. MEYER, FELLOW, IEEE

(*Invited Paper*)

Abstract—This paper presents an overview of current design techniques for operational amplifiers implemented in CMOS and NMOS technology at a tutorial level. Primary emphasis is placed on CMOS amplifiers because of their more widespread use. Factors affecting voltage gain, input noise, offsets, common mode and power supply rejection, power dissipation, and transient response are considered for the traditional bipolar-derived two-stage architecture. Alternative circuit approaches for optimization of particular performance aspects are summarized, and examples are given.

I. INTRODUCTION

THE rapid increase in chip complexity which has occurred over the past few years has created the need to implement complete analog–digital subsystems on the same integrated circuit using the same technology. For this reason, implementation of analog functions in MOS technology has become increasingly important, and great strides have been made in recent years in implementing functions such as high-speed DAC's, sampled data analog filters, voltage references, instrumentation amplifiers, and so forth in CMOS and NMOS technology [1]. These developments have been well documented in the literature. Another key technical development has been a maturing of the state of the art in the implementation of operational amplifiers (op amps) in MOS technology. These amplifiers are key elements of most analog subsystems, particularly in switched capacitor filters, and the performance of many systems is strongly influenced by op amp performance. Many of the developments in MOS operational amplifier design have not been as well documented in the literature, and the intent of this paper is to review the state of the art in this field. This paper is focused on the design of op amps for use within single-chip analog–digital LSI systems, and the particular problems of the design of stand-alone CMOS amplifiers are not addressed.

In Section II, the important performance requirements and objectives for operational amplifiers within a monolithic analog subsystem are summarized. In Section III, the performance of the basic two-stage CMOS operational amplifier architecture is summarized. In Section IV, alternative circuit approaches for the improvement of particular performance aspects are considered. In Section V, the particular problems associated with NMOS depletion load amplifier design are considered, and in Section VI, the design of output stages is considered. Finally, a summary and discussion of the design of amplifiers in scaled technologies are presented in Section VII.

II. PERFORMANCE OBJECTIVES FOR MOS OPERATIONAL AMPLIFIERS

The performance objectives for operational amplifiers to be used within a monolithic analog subsystem are often quite different from those of traditional stand-alone bipolar amplifiers. Perhaps the most important difference is the fact that for many of the amplifiers in the system, the load which the output of the amplifier has to drive is well defined, and is often purely capacitive with values of a few picofarads. In contrast, stand-alone general-purpose amplifiers usually must be designed to achieve a certain level of performance independent of loading over capacitive loads up to several hundred picofarads and resistive loads down to 2 kΩ or less. Within a monolithic analog subsystem, only a few of the amplifiers must drive a signal off chip where the capacitive and resistive loads are significant and variable. In this paper, these amplifiers will be termed output buffers, and the amplifiers whose outputs do not go off chip will be termed internal amplifiers. The particular problems of the design of these output buffers are considered in Section VII.

A typical application of an internal operational amplifier, a switched capacitor integrator, is illustrated in Fig. 1. The basic function of the op amp is to produce an updated value of the output in response to a switching event at the input in which the sampling capacitor is charged from the source and discharged into the summing node. The output must assume the new updated value within the required accuracy, typically on the order of 0.1 percent, within one clock period, typically on the order of 1 μs for voiceband filters. Important performance
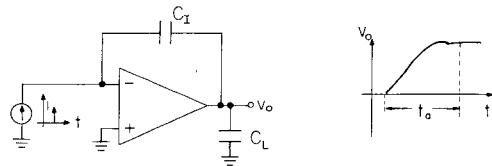
Fig. 1. Typical application of an internal MOS operational amplifier, a switched capacitor integrator.

TABLE I
TYPICAL PERFORMANCE, CONVENTIONAL TWO-STAGE CMOS
INTERNAL OPERATIONAL AMPLIFIER
($+/-5$ V SUPPLY, 4 μm SI GATE CMOS)

dc gain (capacitive load only)	5000
Setting time, 1 V step, C_l = 5 pF	500 ns
Equiv. input noise, 1 kHz	100 nV/$\sqrt{\text{Hz}}$
PSRR, dc	90 dB
PSRR, 1 kHz	60 dB
PSRR, 50 kHz	40 dB
Supply capacitance	1 fF
Power dissipation	0.5 mW
Unity-gain frequency	4 MHz
Die area	75 mils^2
Systematic offset	0.1 mV
Random offset std. deviation	2 mV
CMRR	80 dB
CM range	within 1 V of supply

parameters are the power dissipation, maximum allowable capacitive load, open-loop voltage gain, output voltage swing, equivalent input flicker noise, equivalent input thermal noise, power supply rejection ratio, supply capacitance (to be defined later), and die area. In this particular application the input offset voltage, common-mode rejection ratio, and common-mode range are less important, but these parameters can be important in other applications. Because of the inherent capacitive sample/hold capability in MOS technology, dc offsets can often be eliminated at the subsystem level, making operational amplifier offsets less important. A typical set of values for the parameters given above for a conventional amplifier design in 4 μm CMOS technology are given in Table I. In the following section, the factors affecting the various performance parameters are evaluated for the most widely used amplifier architecture.

III. BASIC TWO-STAGE CMOS OPERATIONAL AMPLIFIER

Currently, the most widely used circuit approach for the implementation of MOS operational amplifiers is the two-stage configuration shown in Fig. 2(b). This configuration is also widely used in bipolar technology, and the bipolar counterpart is also illustrated in Fig. 2(a). The behavior of this circuit when implemented in bipolar technology has been reviewed in an overview article published earlier [2]. This circuit configuration provides good common mode range, output swing, voltage gain, and CMRR in a simple circuit that can be compensated with a single pole-splitting capacitor. While the implementation of this architecture in NMOS technology requires additional circuit elements because of the lack of a complementary device, many NMOS amplifiers commercially manufactured at the present time use a conceptually similar
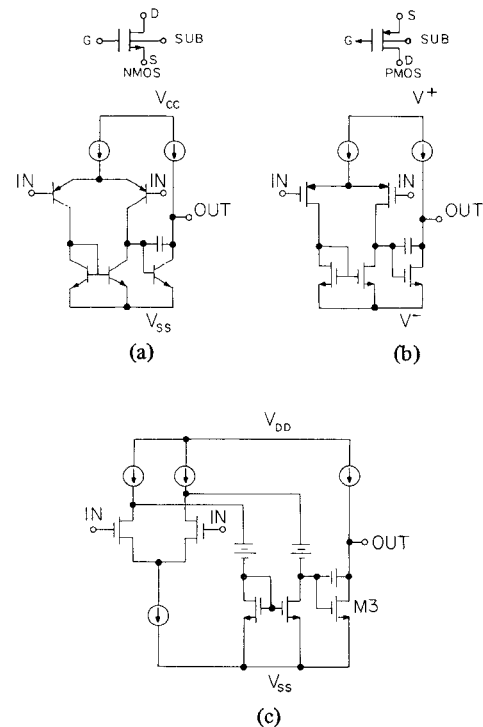

Fig. 2. Two-stage operational amplifier architecture. (a) Bipolar implementation. (b) CMOS implementation. (c) An example of an NMOS implementation with interstage coupling network.

configuration, as illustrated in Fig. 2(c) where a differential interstage level-shifting network composed of voltage and current sources has been inserted between the first and second stages so that both stages can utilize n-channel active devices and depletion mode devices as loads. The implementation of this circuit is discussed further in Section V.

In this section, we will analyze the various performance parameters of the CMOS implementation of this circuit, focusing particularly on the aspects which are different from the bipolar case.

Open Circuit Voltage Gain

An important difference between MOS and bipolar technology is the fact that the maximum transistor open circuit voltage gain g_m/g_o is much lower for MOS transistors than for bipolar transistors, typically by a factor on the order of 10–40 for typically used geometries and bias currents [3]. Under certain simplifying assumptions, voltage gain can be shown to be

$$g_m/g_o = \frac{2L}{V_{gs} - V_T} \left(\frac{dx_d}{dV_{ds}}\right)^{-1} \qquad (1)$$

where x_d is the width of the depletion region between the end of the channel and the drain and L is the effective channel length. The expression illustrates several key aspects of MOS devices used as analog amplifiers. First, for constant drain current decreasing either the channel length or width results in a decrease in the gain, the latter because of the fact that V_{gs} increases. This fact, along with noise considerations, usually dictates the minimum size of the transistors that must be used in a given high-gain amplifier application. Usually, this is
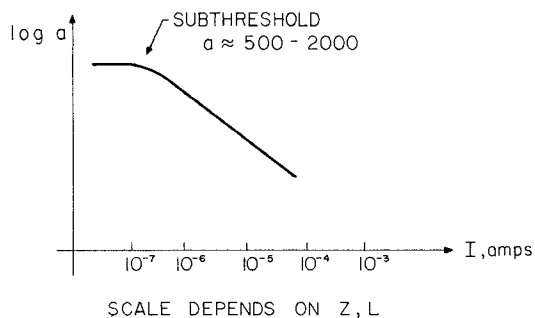
Fig. 3. Typical open circuit gain of an MOS transistor as a function of bias current.
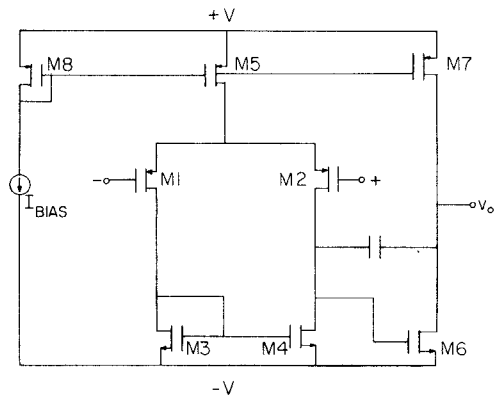

Fig. 4. Schematic of basic two-stage CMOS operational amplifier.

Fig. 5. Typical input offset distribution, MOS operational amplifier.

larger than the length and width used for digital circuits in the same technology.

Second, if the device geometry is kept constant, the voltage gain is inversely proportional to the square root of the drain current since $(V_{gs} - V_T)$ is proportional to the square root of the drain current. A typical variation of open circuit voltage gain as a function of drain current is shown in Fig. 3 [4]. The gain becomes constant at a value comparable to bipolar devices in the subthreshold range of current. This fact makes use of low current levels desirable, and at the same time complicates the design of high-speed amplifiers which must operate at high current.

Third, if device size and bias current are kept constant, the gain is an increasing function of substrate doping since dx_d/dV_{ds} decreases with increasing doping. Thus, devices which have received a channel implant to increase threshold voltage would display a higher open circuit gain than an unimplanted device whose channel doping was lower. Finally, the expression demonstrates that open circuit gain is not degraded by technology scaling in the constant field sense since all terms in the expression decrease in proportion. However, scaling in the quasi-constant field or constant voltage sense would result in a decrease in gain.

Turning to the operational amplifier, the voltage gain of the first stage of the circuit shown in Fig. 4 can be shown to be simply

$$A_{v1} = \frac{g_{m1}}{g_{o2} + g_{o4}} \qquad (2)$$

where g_m is the device transconductance and g_o is the small signal output conductance, and assuming that $M1$ and $M2$ are
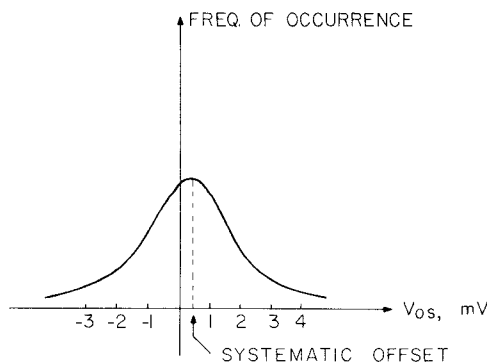
identical and that $M3$ and $M4$ are identical. Similarly, the second stage voltage gain is

$$A_{v2} = \frac{g_{m6}}{g_{o6} + g_{o7}} \cdot \qquad (3)$$

For switched capacitor filter applications, the overall voltage gain required is on the order of several thousand [5], implying a gain in each stage on the order of 50. In order to achieve this level of gain per stage, transistor bias currents and channel lengths and widths are usually chosen such that the transistor $(V_{gs} - V_T)$ is several hundred millivolts, and the drain depletion region is on the order of one fifth or less of the effective channel length at the typical drain bias of several volts. Circuit approaches to achieving more voltage gain or, alternatively, achieving the same voltage gain with smaller devices, are discussed in Section IV.

DC Offsets, DC Biasing, and DC Power Supply Rejection

The input offset voltage of an operational amplifier is composed of two components, the systematic offset and the random offset. The former results from the design of the circuit and is present even when all of the matched devices in the circuit are indeed identical. The latter results from mismatches in supposedly identical pairs of devices. A typical observed distribution of input offset voltages is shown in Fig. 5.

Systematic Offset Voltage

In bipolar technology, the comparatively high voltage gain per stage (on the order of 500) tends to result in a situation in which the input-referred dc offset voltage of an operational amplifier is primarily dependent on the design of the first stage. In MOS op amps, because of the relatively low gain per stage, the offset voltage of the differential to single-ended converter and second stage can play an important role. In Fig. 6, the operational amplifier of Fig. 4 has been split into two separate stages. Assuming perfectly matched devices, if the inputs of the first stage are grounded, then the quiescent output voltage at the drain of $M4$ is equal to the voltage at the drain of $M3$ ($M3$ and $M4$ have the same drain current and gate–source voltage, and hence must have the same drain–source voltage). However, the value of the gate voltage of $M6$ which is required to force the amplifier output voltage to zero may be different from the quiescent output voltage of the first stage. For a first stage gain of 50, for example, each 50 mV difference in these
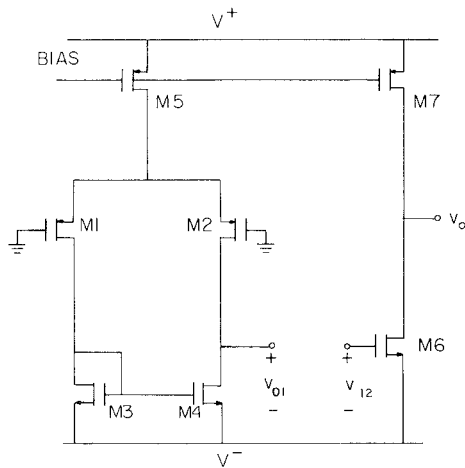
Fig. 6. Two-stage amplifier illustrating interstage coupling constraints.

Fig. 7. Conceptual circuit for calculation of random offset voltage.

voltages results in 1 mV of input-referred systematic offset. Thus, the W/L ratios of $M3, M4$, and $M6$ must be chosen so that the current density in these three devices are equal. For the simple circuit of Fig. 6, this constraint would take the form

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \left(\frac{1}{2}\right)\frac{(W/L)_5}{(W/L)_7}. \tag{4}$$

In order that this ratio be maintained over process-induced variations in channel length, the channel lengths of $M3, M4$, and $M6$ usually must be chosen to be the same, and the ratios provided by properly choosing the channel widths. The use of identical channel lengths for the devices is at odds with the requirements (discussed later) that for low noise, $M3$ and $M4$ have low transconductance, and that for best frequency response under capacitive loading, $M6$ has high transconductance.

Systematic offset voltage is closely correlated with dc power supply rejection ratio. If a systematic offset exists, it is likely to display a dependence on power supply voltage, particularly if the bias reference source is such that the bias currents in the amplifier are not supply independent.

Random Input Offset Voltage

Source-coupled pairs of MOS transistors inherently display somewhat higher input offset voltage than bipolar pairs for the same level of geometric mismatch or process gradient. The reason for this is perhaps best understood intuitively by means of the conceptual circuit shown in Fig. 7. Here, a differential amplifier is made up of an identical pair of unilateral active devices biased at a current I and displaying a transconductance g_m. If the load elements, in this case assumed to be resistors, are assumed to mismatch by a percentage Δ, then in order for the output voltage of the differential amplifier to be zero, the absolute difference in the currents in the two devices must be equal to ΔI. This in turn requires that the dc input difference voltage applied to bring about this difference be

$$V_{gs} = \frac{I}{g_m} \Delta. \tag{5}$$

Thus, the input offset in this case depends on the I/g_m ratio of the active devices and the fractional mismatch in the
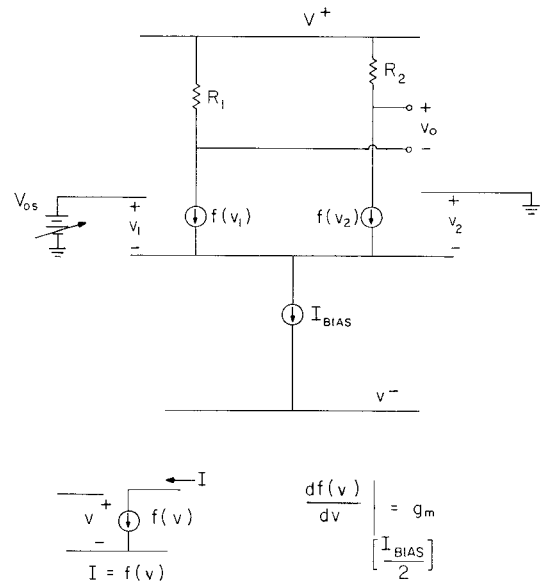
matched elements. A similar dependence is found for mismatches in many of the parameters of the active devices themselves, such as area mismatches in bipolar transistors and channel length and width mismatches in MOS transistors.

For bipolar devices, the I/g_m ratio is equal to kT/q or 0.026 V at room temperature. For MOS transistors, the ratio is $(V_{gs} - V_T)/2$, a bias-dependent quantity which is normally in the 100–500 mV range. While the offset voltage can be substantially improved by operating at low values of V_{gs}, the result is typically a somewhat larger offset voltage than in the bipolar case [2]. As discussed in a later section, the I/g_m ratio also directly effects the slew rate for class A input stages, so that often transient performance requirements place a lower limit on the allowable value of this parameter.

One mismatch component present in MOS devices which is not present in bipolar transistors is the mismatch in the threshold voltage itself. This component does not obey the above relationship, and results in a constant offset component which is bias current independent. Threshold mismatch is a strong function of process cleanliness and uniformity, and can be substantially improved by the use of common centroid geometries. Published data indicate that large-geometry common-centroid structures are capable of achieving threshold match distributions with standard deviations on the order of 2 mV in a silicon gate MOS process of current vintage [6].

Frequency Response, Compensation, Slew Rate, and Power Dissipation

The compensation of the two-stage CMOS amplifier can be carried out much as in the case of its bipolar equivalent using a pole-splitting capacitor C_c as shown in Fig. 2. However, important differences arise because of the much lower transconductance of the MOS transistor relative to bipolar devices [7]. The circuit can be approximately represented by the small-signal equivalent circuit of Fig. 8(a) if the nondominant poles due to the capacitances at the source of $M1$-2, the capacitance at the gate of $M3$, and any other nondominant poles which may exist on the circuit are neglected. This circuit has been analyzed by many authors [2], [8] because it occurs so fre-
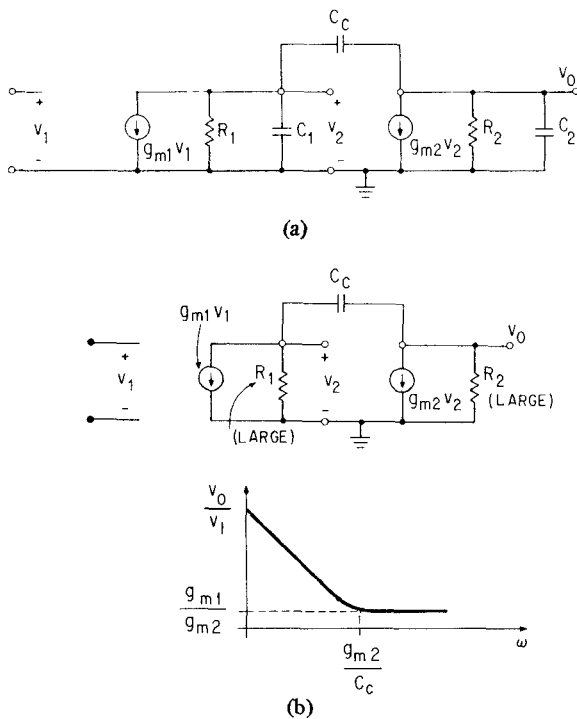
Fig. 8. (a) Small-signal equivalent circuit for two-stage amplifier. (b) Small-signal equivalent circuit with C_1 and C_2 set to zero, and gain of the circuit versus frequency.

quently in bipolar amplifiers. The circuit displays two poles and a right half-plane zero, which under the assumption that the poles are widely spaced, can be shown to be approximately located at

$$p_1 = \frac{-1}{(1 + g_{m2}R_2) C_c R_1} \qquad (6)$$

$$p_2 = \frac{-g_{m2}C_c}{C_2 C_1 + C_2 C_c + C_c C_1} \qquad (7)$$

$$z = + \frac{g_{m2}}{C_c}. \qquad (8)$$

Note that the pole due to the capacitive loading of the first stage by the second, p_1, has been pushed down to a very low frequency by the Miller effect in the second stage, while the pole due to the capacitance at the output node of the second stage, p_2, has been pushed to a very high frequency due to the shunt feedback. For this reason, the compensation technique is called pole splitting.

A unique problem arises when attempting to use pole splitting in MOS amplifiers. Analytically, the problem is illustrated by considering the location of the second pole p_2 and the right half-plane zero z relative to the unity-gain frequency g_{m1}/C_c. Here we make the simplifying assumption that the internal parasitic C_1 is much smaller than either the compensation capacitor C_c or the load capacitance C_2. This gives

$$\left| \frac{p_2}{\omega_1} \right| = \frac{g_{m2}C_c}{g_{m1}C_2} \qquad (9)$$

$$\left| \frac{z}{\omega_1} \right| = \frac{g_{m2}}{g_{m1}}. \qquad (10)$$

Note that the location of the right half-plane zero relative to

the unity-gain frequency is dependent on the ratio of the transconductances of the two stages.

Physically, the zero arises because the compensation capacitor provides a path for the signal to propagate directly through the circuit to the output at high frequencies. Since there is no inversion in that signal path as there is in the inverting path dominant at low frequencies, stability is degraded. The location of the zero can best be conceptually understood by considering a case in which C_1 and C_2 are zero as illustrated in Fig. 8(b). For low frequencies, this circuit behaves like an integrator, but at high frequencies, the compensation capacitor behaves like a short circuit. When this occurs, the second stage behaves like a diode-connected transistor, presenting a load to the first stage equal to $1/g_{m2}$. Thus, the circuit displays a gain at high frequencies which is simply g_{m1}/g_{m2}, as illustrated in Fig. 8(b). The polarity of this gain is opposite to that at low frequencies, turning any negative feedback that might be present around the amplifier into positive feedback.

In bipolar technology, the transconductance of the second stage is normally much higher than the first because it is operated at relatively high current and the transconductance of the bipolar device is proportional to current level. In MOS amplifiers, the transconductances of the two stages tend to be similar, in part because the transconductance varies only as the square root of the drain current. Also, the transconductance of the first stage must be kept reasonably high for thermal noise reasons.

Fortunately, two effective means have evolved for eliminating the effect of the right half-plane zero. One approach has been to insert a source follower in the path from the output back through the compensation capacitor to prevent the propagation of signals forward through the capacitor [7]. This works well, although it requires more devices and dc bias current. An even simpler approach is to insert a nulling resistor in series with the compensation capacitor as shown in Fig. 9 [9]. In this circuit, note that at high frequencies, the output current from the first stage must flow principally as drain current in the second stage transistor. This, in turn, gives rise to voltage variation at the gate of the second stage which is proportional to the small-signal current from the first stage and inversely proportional to the transconductance of the second stage. In the circuit of Fig. 8, this voltage appears directly at the output. However, if a resistor of value equal to $1/g_{m2}$ is inserted in series with the compensation capacitor, the voltage across this resistor will cancel the small-signal voltage appearing on the left side of the compensation capacitor, resulting in the cancellation of the feedthrough effect.

Using an analysis similar to that performed for the circuit of Fig. 8, one obtains pole locations which are close to those for the original circuit, and a zero location of

$$z = \frac{1}{C_c \left(\frac{1}{g_{m2}} - R_z \right)}. \qquad (11)$$

As expected, the zero vanishes when R_z is made equal to $1/g_{m2}$. In fact, the resistor can be further increased to move the zero into the left half-plane to improve the amplifier phase margin [10]. The movement of the zero for increasing values of R_z is illustrated in Fig. 10.
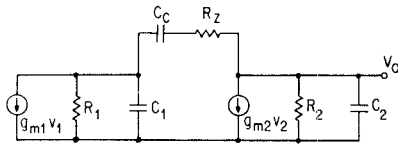
Fig. 9. Small-signal equivalent circuit of the basic amplifier with nulling resistor added in series with the compensation capacitor.
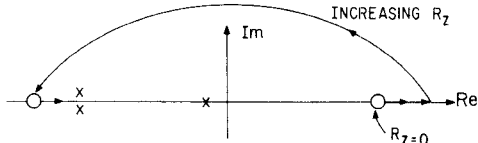

Fig. 10. Pole-zero diagram showing movement of the transmission zero for various values of R_z.

A second problem in compensation involves the effects of capacitive loading. From (9), the location of the nondominant pole due to capacitive loading on the output node relative to the unity-gain frequency is determined by the ratio of the second-stage transconductance to that of the first and the ratio of the load capacitance to the compensation capacitance. Since the stage transconductances tend to be similar, this implies that the use of load capacitances of the same order as the compensation capacitance will tend to degrade the unity-gain phase margin because of the encroachment of this nondominant pole. This is of considerable practical significance in switched capacitor filters where large capacitive loads must be driven, and the use of an output stage is undesirable for power dissipation and noise reasons.

Slew Rate

As in its bipolar counterpart, the CMOS op amp of Fig. 4 displays a relationship among slew rate, bandwidth, input stage bias current, and input device transconductance of

$$SR = \frac{I_{D1}}{g_{m1}} \omega_1 \qquad (12)$$

where g_{m1} is the input transistor transconductance, I_{D1} is the bias current of the input devices, and ω_1 is the unity-gain frequency of the amplifier. For the MOS case, this gives

$$SR = \frac{(V_{gs} - V_T)_1}{2} \omega_1. \qquad (13)$$

In effect, the $(V_{gs} - V_T)$ of the input stage is the range of differential input voltage for which the input stage stays in the active region. If the bandwidth is kept constant and this range is increased, the slew rate improves. Because this range is usually substantially higher in MOS amplifiers than in bipolar amplifiers, MOS amplifiers usually display relatively good slew rate. In micropower or precision applications where the input transistors are operated at very low $(V_{gs} - V_T)$, this may not be the case, however.

Power Dissipation

Even for the simple circuit of Fig. 4, the minimum achievable power dissipation is a complex function of the technology used and the particular requirements of the application. In

sampled data systems such as switched capacitor filters, the requirement is that the amplifier be able to settle in a certain time to a certain accuracy with a capacitive load of several picofarads. In this application, the factors determining the minimum power dissipation tend to be the fact that there must be enough standing current in the amplifier class A second stage such that the capacitance can be charged in the allowed time, and the fact that the amplifier must have sufficient phase margin to avoid degradation of the settling time due to ringing and overshoot. The latter requirement dictates a certain minimum g_m in transistor $M6$ for a given bandwidth and load capacitor. This, in turn, usually dictates a certain minimum bias current in $M6$ for a reasonable device size. If a class A source follower output stage is added, then the same comment would apply to its bias current since its g_m, together with the load capacitance, contribute a nondominant pole.

The preceding discussion is predicted on the use of class A circuitry (i.e., circuits whose available output current is not greater than the quiescent bias current). Quiescent power dissipation can be greatly reduced through the use of dynamic circuits and class B circuits, as discussed later.

Noise Performance

Because of the fact that MOS devices display relatively high $1/f$ noise, the noise performance is an important design consideration in MOS amplifiers. All four transistors in the input stage contribute to the equivalent input noise, as illustrated in Fig. 11. By simply calculating the output noise for each circuit and equating them (11),

$$V_{eqTOT}^2 = V_{eq1}^2 + V_{eq2}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)(V_{eq3}^2 + V_{eq4}^2) \qquad (14)$$

where it has been assumed that $g_{m1} = g_{m2}$ and that $g_{m3} = g_{m4}$. Thus, the input transistors contribute to the input noise directly, while the contribution of the loads is reduced by the square of the ratio of their transconductance to that of the input transistors. The significance of this in the design can be further appreciated by considering the input-referred $1/f$ noise and the input-referred thermal noise separately.

Input-Referred 1/f Noise

The equivalent input noise spectrum of a typical MOS transistor is shown in Fig. 12. The dependence of the $1/f$ portion of the spectrum on device geometry and bias conditions has been studied by many authors [12]-[14]. Considerable discrepancy exists in the published data on $1/f$ noise, indicating that it arises from a mechanism that is strongly affected by details of device fabrication. Perhaps the most widely accepted model for $1/f$ noise is that for a given device, the gate-referred equivalent mean-squared voltage noise is approximately independent of bias conditions in saturation, and is inversely proportional to the gate capacitance of the device. The following analytical results are based on this model, but it should be emphasized that the actual dependence must be verified for each process technology and device type [12], [15]. Thus,

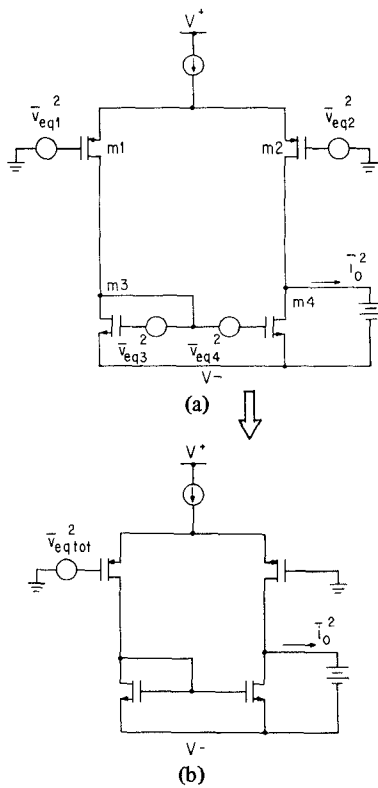$$V_{1/f}^2 = \frac{K}{C_{ox}WL} \left(\frac{\delta f}{f}\right). \qquad (15)$$

Fig. 11. CMOS input stage. (a) Device noise contributions. (b) Equivalent input noise.
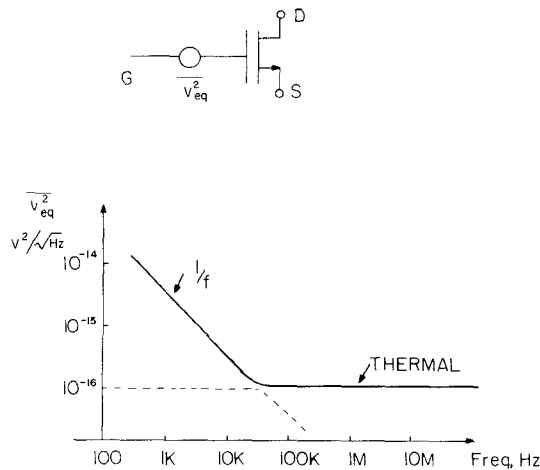

Fig. 12. Typical equivalent input noise, MOS transistor.

Utilizing this assumption, we obtain for the equivalent input noise

$$V_{1/f}^2 = \frac{2K_p}{W_1 L_1 C_{ox}} \left(1 + \frac{K_n \mu_n L_1^2}{K_p \mu_p L_3^2}\right)\left(\frac{\delta f}{f}\right) \tag{16}$$

where K_n and K_p are the flicker noise coefficients for the n-channel and p-channel devices, respectively. Depending on processing details, these may be comparable or different by a factor of two or more. Note that the multiplying term in front is the input noise of the input transistors, and the second term is the increase in noise due to the loads. It is clear from this second term that the load contribution can be made small by simply making the channel lengths of the loads longer than

that of the input transistors by a factor of on the order of two or more. The input transistors can then be made wide enough to achieve the desired performance. It is interesting to note that increasing the width of the channel in the loads does not improve the $1/f$ noise performance.

Thermal Noise Performance

The input-referred thermal noise of an MOS transistor is given by [8]

$$V_{eq}^2 = 4kT\left(\frac{2}{3g_m}\right)\delta f. \tag{17a}$$

Utilizing the same approach as for the flicker noise, this gives

$$V_{eq}^2 = 4kT \ \frac{4}{3\sqrt{2\mu_p C_{ox}(W/L)_1 I_D}} \left(1 + \sqrt{\frac{\mu_n(W/L)_3}{\mu_p(W/L)_1}}\right). \tag{17b}$$

Again, the first term represents the thermal noise from the input transistors, and the term in parentheses represents the fractional increase in noise due to the loads. The term in parentheses will be small if the W/L's are chosen so that the transconductance of the input devices is much larger than that of the loads. If this condition is satisfied, then the input noise is simply determined by the transconductance of the input transistors.

Power Supply Rejection and Supply Capacitance

Power supply rejection ratio (PSRR) is a parameter of considerable importance in MOS amplifier design. One reason for this is that in complex analog–digital systems, the analog circuitry must coexist on the same chip with large amounts of digital circuitry. Even though separate analog and digital supply buses are often run on chip, it is hard to avoid some coupling of digital noise into the analog supplies. A second reason is that in many systems, switching regulators are used which introduce power supply noise into the supply voltage lines. If these high-frequency signals couple into the signal path in a sampled data system such as a switched capacitor filter or high-speed A/D converter, they can be aliased down into the frequency band where the signal resides and degrade the overall system signal-to-noise ratio. The parameters reflecting susceptibility to this phenomenon in the operational amplifier are the high-frequency PSRR and the supply capacitance.

The PSRR of an operational amplifier is simply the ratio of the voltage gain from the input to the output (open loop) to that from the supply to the output. It can be easily demonstrated that for frequencies less than the unity-gain frequency, if the operational amplifier is connected in a follower configuration and an ac signal is superimposed on one of the power supplies, the signal appearing at the output is equal to the applied signal divided by the PSRR for that supply. The basic circuit of Fig. 4 is particularly poor in terms of its high-frequency rejection from the negative power supply, as illustrated in Fig. 13. The primary reason is that as the applied frequency increases, the impedence of the compensation capacitor decreases, effectively shorting the drain of $M6$ to its gate for ac signals. Thus, the gain from the negative supply to the output

$$PSRR^+ = \left| \frac{\left\{ \frac{V_o}{V_i}(\omega) \right\}}{\left\{ \frac{V_o}{V^+}(\omega) \right\}} \right|$$

$$PSRR^- = \left| \frac{\left\{ \frac{V_o}{V_i}(\omega) \right\}}{\left\{ \frac{V_o}{V^+}(\omega) \right\}} \right|$$
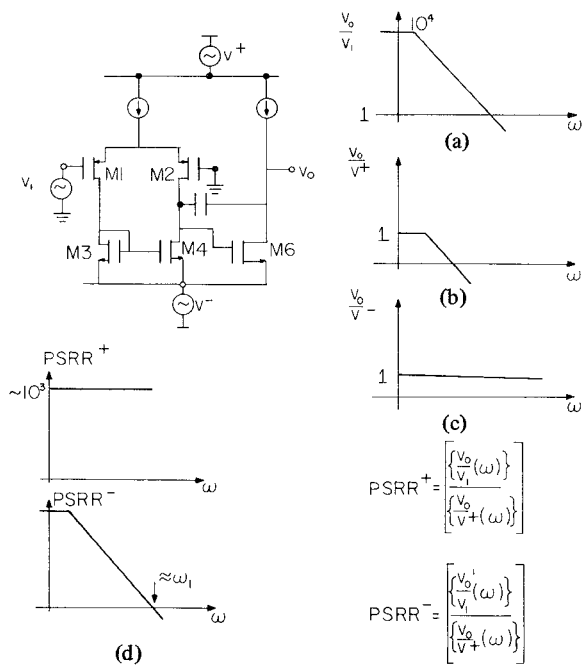
Fig. 13. High-frequency PSRR of bipolar-derived op amp. (a) Gain from input to output. (b) Gain from positive supply to output. (c) Gain from negative supply to output. (d) Positive and negative PSRR.

Fig. 14. Supply capacitance in a CMOS amplifier.

approaches unity and stays there out to very high frequencies. The same phenomenon causes the gain from the positive supply to fall with frequency as the open-loop gain does, so that the positive PSRR remains relatively flat with increasing frequency. The negative supply PSRR falls to approximately unity at the unity-gain frequency of the operational amplifier. Several alternative amplifier architectures have evolved which alleviate this problem, and they are discussed in a later section.

A second important contribution to coupling between the power supply and the signal path at high frequency is termed supply capacitance [10], [17]. This phenomenon manifests itself as a capacitive coupling between one or both of the power supplies and the operational amplifier input leads. The effect of this capacitance is illustrated in Fig. 14 for a switched capacitor integrator. Since the op amp input is connected to the summing node, then the power supply variations will appear at the integrator output attenuated by the ratio of the supply capacitance to the integrator capacitance. The result can be quite poor power supply rejection in switched capacitor filters and other sampled data analog circuits.

Supply capacitance effects can occur in several ways, but four important ones are given below.

1) Variation in drain voltage on $M1, M2$ with negative supply voltage. If the op amp inputs are grounded and the negative supply voltage changes, then a displacement current flows into the summing node because of the resulting change in voltage across the drain-gate capacitance of the input transistors. This is usually eliminated by the use of cascode transistors in series with the drains of the input transistors.

2) Variation of drain current in $M1, M2$ with supply voltage. Use of a bias reference which results in bias current variations with supply voltage will, in turn, cause the $V_{gs} - V_T$ of the input devices to change with supply voltage. This will cause a
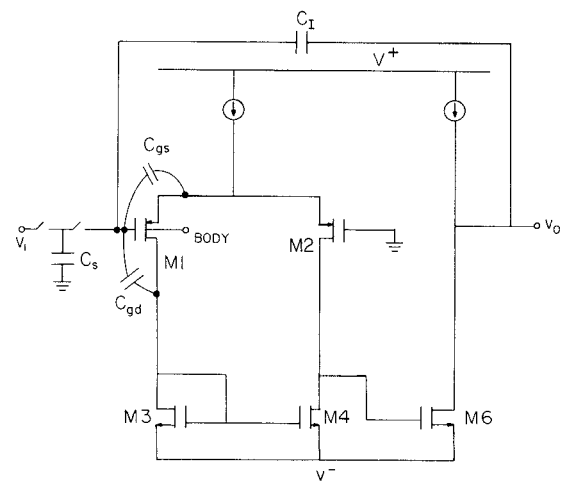
displacement current to flow through the gate-source capacitance of $M1, M2$ onto the summing node. The usual solution to this problem is the use of a supply-independent bias reference.

3) Variation of body bias on $M1, M2$ with supply voltage variations. If the substrate terminal of the input transistors is tied to a supply or supply-related voltage, then as the supply voltage changes, the substrate bias changes. This, in turn, changes the threshold, which changes V_{gs}. The resulting displacement current in C_{gs} flows into the summing node. In CMOS operational amplifiers, the usual solution to this problem is to put the input transistors in a well and tie the well to the sources of the input transistors. This dictates, for example, that in a p-well process, the input devices be n-channel devices, and vice versa. In NMOS, the use of fully differential circuitry is probably the only way to fully alleviate the problem since the substrate must be tied to a supply. A second alternative is capacitive decoupling of the substrate so that it does not follow high-frequency supply variations [17].

4) Interconnect crossovers in the amplifier layout and in the system layout can produce undesired supply capacitance. This can usually be overcome with careful layout.

IV. ALTERNATIVE ARCHITECTURES FOR IMPROVED PERFORMANCE

The bipolar-derived amplifier discussed above is widely used at the present time, although with many variations, in a variety of applications. However, many alternative circuit approaches have been investigated and, in many cases, utilized in commercial products in order to achieve performance which is superior to that available from the basic circuit in some respect. In this section, we first consider variations on the basic circuit, and then alternative architectures.

Variations on the Basic Two-Stage Amplifier

Use of Cascodes for Improved Voltage Gain: In precision applications involving large values of closed-loop gain, the voltage gain available from the basic circuit shown in Fig. 4 may be inadequate. One approach to improving the voltage gain without adding an additional common-source stage with its
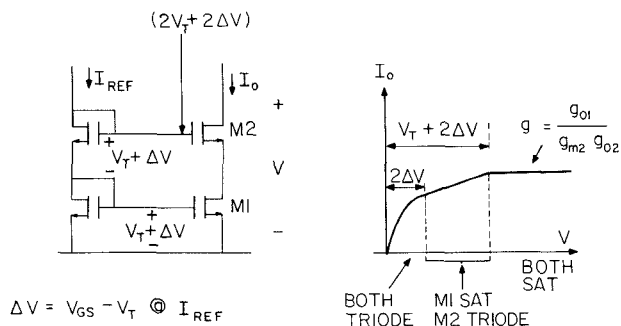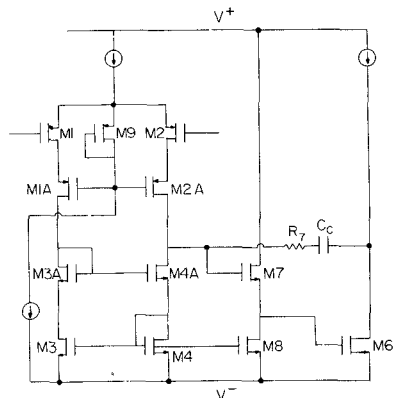
Fig. 15. Cascode current source.

Fig. 16. Two-stage amplifier with cascoded first stage.

Fig. 17. Schematic of basic amplifier with cascode feedback compensation.

associated high impedence node and pole is to add a common-gate, or cascode, transistor to increase the output resistance of the common-source transistors in the basic amplifier. The basic cascode circuit is shown in Fig. 15. It is easily demonstrated that the incremental output resistance of this current source is equal to

$$r_o = r_{o2}[1 + g_{m2}r_{o1}] + r_{o1}. \tag{18}$$

The output resistance is increased by an amount equal to the open circuit gain of the cascode transistor. This circuit may be directly applied to the basic two-stage amplifier in either the first stage, second stage, or in both stages. The circuit of Fig. 16 illustrates the use of cascodes in the first stage. One disadvantage of this circuit is a substantial reduction in input stage common mode range, but this can be alleviated by optimizing the biasing of the cascodes, to be discussed in Section V.

Improved PSRR Grounded-Gate Cascode Compensation: Read and Wieser [18] have recently described a technique for improving the negative supply PSRR of the circuit of Fig. 4. Conceptually, if the left end of the capacitor could be connected to a virtual ground, then the capacitor voltage would not have to change whenever the negative supply voltage changed in order to have the output remain constant. This was accomplished by inserting a cascode device in this loop with the gate connected to ground, as shown in Fig. 17. The displacement current from the capacitor flows into the source of this transistor and out the drain into the compensation point. An additional current source and current sink of equal values must be added to bias the common-gate device in the active region and so as not to contribute any systematic offset.
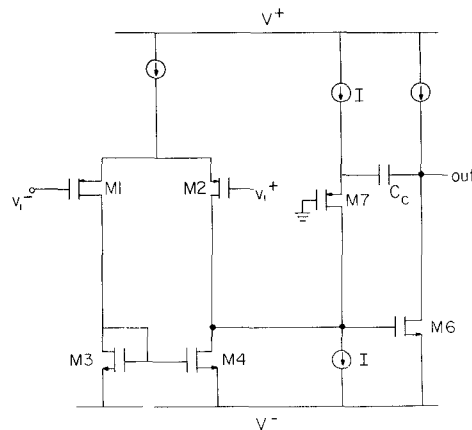
The resulting negative PSRR at high frequencies is greatly improved at the cost of a slight increase in complexity, random offset, and noise [16].

Common-Source Common-Gate Amplifiers

The basic amplifier considered thus far is actually a cascade of two common-source stages. An alternative approach is to use a cascade of a common-source stage and a common-gate stage, often called a cascode amplifier. An example of an amplifier utilizing this architecture is shown in Fig. 18. The voltage gain of this circuit at dc is approximately the same as that of the basic two-stage circuit. The small-signal impedance at the output node is increased by $g_m r_o$ relative to the output node of the two-stage circuit, and the voltage gain is simply the product of the transconductance of the input transistors and the impedance at the output mode:

$$A_v = \frac{g_{m1}}{\dfrac{g_{o2} + g_{o9}}{g_{m4}r_{o4}} + \dfrac{g_{o7}}{g_{m5}r_{o5}}}. \tag{19a}$$

The principal reasons for considering this architecture are twofold. First, the compensation capacitor and load capacitor are the same element in this circuit. The first nondominant pole comes from the g_m/C_{gs} time constant of the n-channel cascode devices, and gives a pole frequency approximately at the f_t of these devices. A second nondominant pole results from the differential to single-ended converter. However, the nondominant pole due to the load capacitance present in the two-stage circuit, is not present in this circuit. Thus, this circuit is capable of achieving higher stable closed-loop bandwidth with large capacitive load. The principal application of this architecture to date has been in high-frequency switched capacitor filters [20], [21].

An important advantage of this circuit is that it does not suffer from the degradation of the high-frequency power supply rejection problem inherent in the pole-split compensated two-stage architecture, assuming that the load capacitance or part of it is not tied to a power supply.

Because of the fact that cascode transistors are used at the output, the output swing of this circuit is lower than the common-source common-source amplifier. This problem can
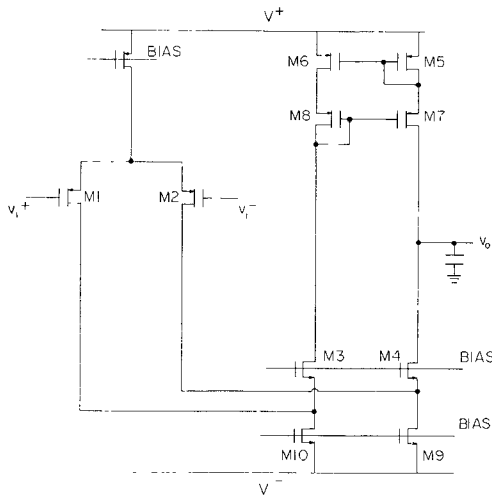
Fig. 18. One-stage amplifier schematic.

Fig. 19. Example circuit illustrating class AB second stage.

be minimized by modifying the bias generator such that the lower transistors in the cascode current source are biased on the edge of saturation (i.e., $V_{gd} = V_T$). This results in an available output voltage swing within $2(V_{gs} - V_T)$ of each supply, or perhaps 0.4 to 0.8 V in voiceband filters. MOS transistors actually display a rather indistinct transition from triode to saturation as the drain depletion region forms, and as a result, the bias point must actually be chosen so as to bias the lower transistor a few hundred millivolts into saturation if the predicted value of incremental output resistance is to be obtained.

A second disadvantage of this circuit is that more devices contribute to the input-referred voltage and input offset voltage. Assuming that transistors $M5$-$M8$ are biased at the same current as the input devices, the input-referred flicker noise can be shown to be

$$v_{eq}^2 = \frac{2K_p}{W_1 L_1} \left[1 + \frac{2K_n \mu_n}{K_p \mu_p} \left(\frac{L_1}{L_9} \right)^2 + \left(\frac{L_1}{L_5} \right)^2 \right] \frac{\delta f}{f}. \qquad (19b)$$

In this case, the current sources $M9$ and $M10$ contribute an additional term not present in (16). However, as in the case of the common-source common-source amplifier, the equivalent input noise can be made almost equivalent to the noise of the input transistors alone by choosing the channel lengths of the input transistors to be short compared to those of $M5$, $M6$, $M9$, and $M10$. The same considerations apply for the thermal noise.

Class AB Amplifiers, Dynamic Amplifiers, and Dynamic Biasing

Many, if not all, MOS analog circuits commercially produced utilize class AB circuitry in some form. Here the term class AB is taken to mean a circuit which can source and sink current from a load which is larger than the dc quiescent current flowing in the circuit. The most widespread application is in output buffers, but if an important objective is the minimization of chip power, then the philosophy of using class AB operation can be extended to the internal amplifiers. The motivation for doing so is that one of the factors that dictates the value of the quiescent current with an MOS amplifier is the
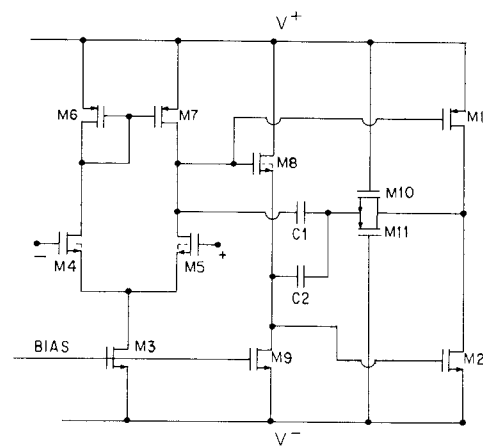
value of current required to charge the load and/or the compensation capacitance in the required time. However, it is relatively rare that the operational amplifier outputs actually have to change the maximum amount in one clock cycle. Large power savings can be effected if only that current is drawn which is required to charge the capacitance on that particular cycle. An example of an amplifier utilizing a class A first stage and a class AB second stage is shown in Fig. 19 [22]. In a conventional circuit, the gate of $M2$ would be connected to a level-shifted version of the stage input voltage. Thus, when the first stage output swings positive, reducing the current in $M1$, the current in $M2$ increases above its quiescent dc value. An example of a single-stage amplifier that operates on this principle is shown in Fig. 20 [23]. This particular circuit can be used in the inverting mode only. With the input grounded, the quiescent current in the input transistors is determined by the bias voltages shown. Upon the application of a voltage to the input, the current in one side of the input stage increases monotonically with the applied voltage until the power supply is reached, while the other side of the input stage turns off. The amount of current available at the output is much larger than the quiescent current, and the circuit, as a result, does not follow the relationship of (12). In fact, the circuit does not display slew rate limiting in the usual sense. Another aspect of this circuit is the fact that the small-signal voltage gain in the quiescent mode can be quite high because of the low current level, and the fact that the voltage gain falls off during transients because of the high current levels is of little consequence. Similar circuits have been used extensively in bipolar technology [24].

Degrauwe et al. [25] have recently described a novel approach to the same objective. A conventional class A amplifier configuration is used, but an auxiliary circuit is used to detect the presence of large differential signals at the input. The bias current in the class A circuitry is then increased when such signals are present. Experimental versions of such amplifiers have yielded quiescent power dissipation of less than 10 μW.

A second class of amplifiers has been explored by several authors, beginning with Copeland [26], in which the quiescent current in the absence of signals is allowed to decay to zero. Such amplifiers are fully dynamic in the sense that no dc paths
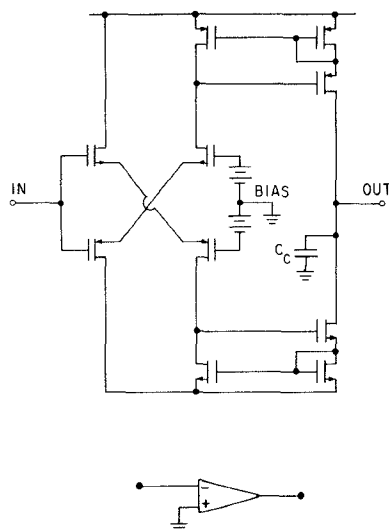
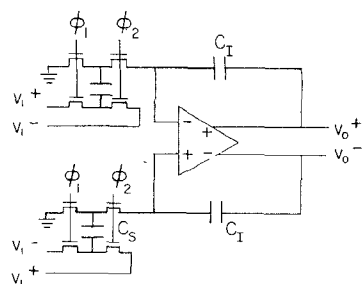Fig. 20. Examples of a single-stage class AB op amp.

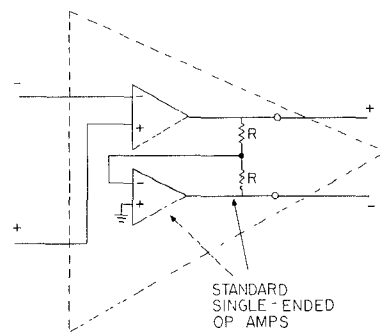Fig. 21. Differential switched capacitor integrator.

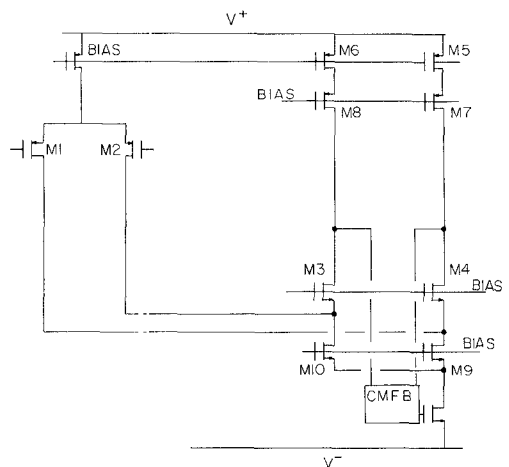Fig. 22. Equivalent circuit for a differential output operational amplifier.

Fig. 23. Example of a differential output amplifier. The block labeled $CMFB$ serves to keep the common-mode output voltage near ground.

exist for current to flow from the supply. While very low values of power dissipation can be obtained, difficult problems of settling time and power supply rejection remain to be solved with these amplifiers.

Hostica [27] has described a third approach to micropower amplifier design for switched capacitor applications which utilizes a time-varying periodic bias current which is synchronous with the master clock in the filter. In contrast to the approaches described above, the power supply current is independent of signal amplitude, and is made large during the early part of the clock period for fast slewing and small during the later portion for high gain and power savings. The bias current waveform is generated by discharging a capacitor into the input of a current mirror. While this technique, in principle, dissipates more power than the other approaches under low signal conditions, it can be implemented with relatively simple circuitry, and it has demonstrated good experimental results for both one-stage and two-stage amplifiers [28].

V. DIFFERENTIAL OUTPUT AMPLIFIERS

As has been mentioned, power supply rejection is an important performance parameter for amplifiers to be used in complex analog/digital systems. In addition, one inevitable result of technology scaling is a reduction in power supply voltage with an accompanying reduction in internal signal swings and dynamic range. These two considerations make use of fully differential signal paths throughout the analog portions of the system attractive for some systems [29], [30]. The inherently differential nature of the circuit tends to give very high PSRR since the supply variations appear as a common mode signal. Also, the effective output swing is doubled, while the magnitude of the input-referred operational amplifier noise remains the same, giving a 6 dB improvement in operational amplifier noise-limited dynamic range.

A typical implementation of a differential switched capacitor integrator is shown in Fig. 21. The operational amplifier is required to produce two analog outputs which are symmetric about ground, in contrast to the single-ended case where only one is produced. An equivalent circuit for a differential op

amp is shown in Fig. 22. An example of a CMOS differential output operational amplifier is shown in Fig. 23.

An important problem in such amplifiers is the design of a feedback loop to force the common mode output voltage to be ground or some other internal reference potential. This feedback path can be implemented with transistors in a continuous-time circuit or can be implemented with switched capacitor circuitry. The continuous approach is potentially simpler, but presents a difficult design problem in making the common-mode output voltage independent of the differential mode signal voltage [21], [29]. Switched capacitor circuitry can make use of the linearity of MOS capacitors to achieve this goal [30]. The choice between the two techniques depends on the sensitivity of the particular application to variations in common-mode voltage.
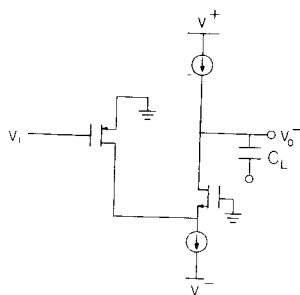
Fig. 24. Small-signal differential half circuit for the amplifier in Fig. 23.

Another important advantage of differential output amplifiers is that the differential single-ended converter with its associated nondominant poles is eliminated. The small-signal equivalent circuit for the circuit in Fig. 22, for example, is a simple common-source common-gate cascade, as shown in Fig. 24. This circuit has only one nondominant pole, at the f_t of the common-gate device. Thus the configuration is particularly well suited to the implementation of high-frequency switched capacitor filters. A configuration of this type has been used in recently reported work yielding high-Q switched capacitor filters clocked at 4 MHz with center frequencies of 250 kHz in a 4 μm silicon gate CMOS technology [21].

VI. NMOS OPERATIONAL AMPLIFIERS

The design of an operational amplifier of a given performance level in NMOS depletion load technology is a much more difficult task than in CMOS technology. The absence of a complementary device makes the implementation of level shifters which track supply voltage variations much more complex. The level of body effect found in most depletion load devices makes the realization of large gains per stage difficult. Assuming that the basic architecture is similar to that illustrated in Fig. 2(c), the small-signal properties, voltage gain, transient response and slew rate, input noise, and power supply rejection considerations are basically similar to the two-stage CMOS amplifier. The key additional considerations are the shunting effects of the incremental output conductance of the depletion load current sources and the impedance and power supply variation of the floating level-shifting voltage sources and the resulting degradation of power supply rejection ratio. Nonetheless, creative circuit design has resulted in NMOS amplifiers which nearly match CMOS amplifiers in most performance aspects, albeit at the cost of somewhat more complexity, die area, and power dissipation. Circuit techniques used to achieve this include replica biasing for tracking level shifters [9], [17], positive feedback for high voltage gain [31], [30], differential configurations for power supply rejection [29], [30], and others.

While there will no doubt always be a need for NMOS amplifiers for some applications, the emergence of CMOS as a key VLSI digital technology has resulted in the widespread adoption of CMOS for new mixed analog–digital designs.

VII. OUTPUT BUFFERS

In amplifier applications involving either a large capacitive or resistive load, an output stage must be added to the basic am-plifier to prevent the load from degrading the voltage gain or closed-loop stability. This situation most often arises when signals must be supplied off the chip to an external environment. The key requirements on such stages is that they be sufficiently broad band with heavy capacitive loading such that they do not degrade the loop stability of the operational amplifier, and such that the output is able to supply a large enough voltage swing to the load with the maximum load conductance. While class A source follower or emitter follower circuits can be used in some applications, quiescent power dissipation considerations usually dictate a class AB implementation of the circuit. This discussion is limited to class AB output buffers.

In bipolar operational amplifier design, the complementary emitter follower class AB configuration is used in the vast majority of cases. In contrast, class AB CMOS output stage implementations tend to vary widely, depending on the specific devices available in the particular technology used. The CMOS complementary source follower class AB output buffer stage shown in Fig. 25 is a direct analog of its bipolar counterpart. The primary drawback of this circuit is that the output voltage swing is limited by the gate–source voltage of the output transistors. This occurs because the transistors used for logic functions on the chip have thresholds in the 0.5–1 V range, so that the amount of swing lost due to threshold voltage plus the $(V_{gs} - V_T)$ drop is too large for many applications. However, many technologies have an extra device type with very low threshold voltage, and in this case, this low threshold device can be used for one of the two output transistors. It is rare that both p-channel and n-channel low threshold devices are available in the same technology.

In many CMOS technologies, a bipolar transistor follower is available and can be used in place of one of the output followers. This provides very low output resistance and good output swing. In processes with light substrate doping, potential latchup problems can make the use of such devices in off-chip driver stages impractical because of the fact that the collector current of the transistor flows in the substrate and can cause voltage drops which cause a junction to be forward biased. An example of the use of a bipolar device in an MOS output stage together with a low threshold device is illustrated in Fig. 26.

A third alternative is the use of quasi-complementary configurations in which a common-source transistor together with an error amplifier is used in place of one or both of the follower devices. This circuit is shown conceptually in Fig. 27. The combination of the error amplifier and the common-source device mimics the behavior of a follower with high dc transconductance. Such quasi-complementary circuits provide excellent dc performance with voltage swings approaching the supply rails, but since the amplifier must be broad band to prevent crossover distortion problems, they present difficult problems in compensation of the local feedback loop in the presence of large capacitive loads. Proper control of the quiescent current is also a key design constraint.

Low threshold devices, bipolar devices, and quasi-complementary devices can be used in any combination, depending on what devices are available in the particular technology
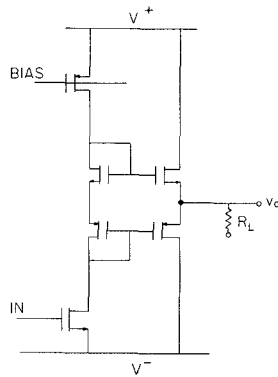
Fig. 25. Complementary source follower CMOS output stage based on the traditional bipolar implementation.
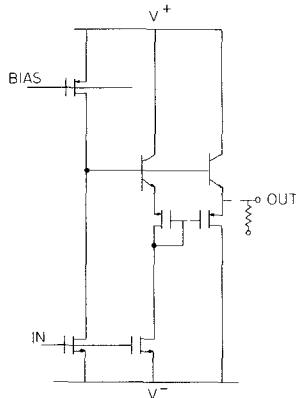

Fig. 26. Example of a CMOS output stage using a bipolar emitter follower and a low-threshold p-channel source follower.
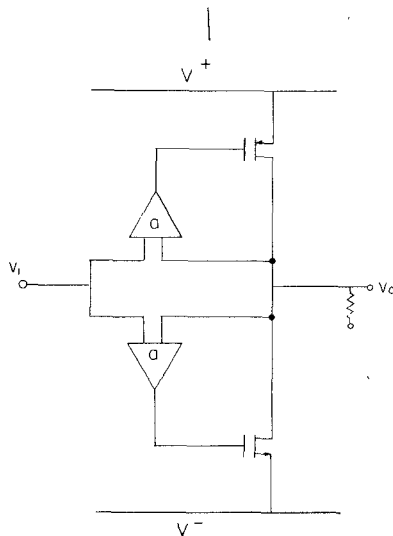

Fig. 27. Example of a complementary class B output stage using compound devices with imbedded common-source output transistors.

being used. Whereas in the bipolar case the vast majority of output stage applications can be satisfied using the traditional complementary class B emitter follower stage, no single circuit approach has yet emerged as the standard for CMOS output stages.

VIII. SUMMARY AND CONCLUSIONS

In this paper, we have attempted to summarize the various techniques and architectures which have been applied in the

design of MOS operational amplifiers in the past several years. An important question is the extent to which these amplifier designs can be scaled as minimum feature sizes continue to decrease. As pointed out in a recent study [32], dc parameters such as voltage gain are generally unaffected for constant-field scaling, although they are degraded for quasi-constant voltage or constant voltage scaling. Perhaps the most difficult problem results from the fact that the effective dynamic range of the amplifier falls in scaled technologies. This occurs fundamentally because of the fact that analog signal swings fall with reductions in power supply voltage. Input-referred thermal noise remains constant because of the fact that the device transconductance remains constant under constant-field scaling. The input-referred $1/f$ noise increases, but this does not appear to be a fundamental limitation on system dynamic range because the signal can always be translated to a higher portion of the spectrum using techniques like chopper stabilization [29]. Also, newer technologies have demonstrated continuing reductions in $1/f$ noise as a result of better process control.

In sampled data analog amplifiers, filters and data converters, the primary limitation on dynamic range, assuming that $1/f$ noise has been removed, is the kT/C noise contributed by the analog switches making up the filter. The kT/C limited dynamic range also falls as the technology is scaled, and since for practical clock rates and capacitor sizes this noise source is dominant over op amp thermal noise, there appears to be no barrier to constant-field scaling of operational amplifiers for this application, assuming that $1/f$ noise is removed by circuit or technological means. Thus, the adaptation of the circuit approaches described in this paper to lower supply voltages and scaled devices, and the removal of $1/f$ noise from the signal path in such circuits, are important objectives in future work.

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Paul R. Gray (S'56–M'69–SM'76–F'81), for a photograph and biography, see p. 419 of the April 1982 issue of this JOURNAL.

Robert G. Meyer (S'64–M'68–SM'74–F'81) was born in Melbourne, Australia, on July 21, 1942. He received the B.E., M.Eng.Sci., and Ph.D. degrees in electrical engineering from the University of Melbourne, Melbourne, Australia, in 1963, 1965, and 1968, respectively.

In 1968 he was employed as an Assistant Lecturer in Electrical Engineering at the University of Melbourne. Since September 1968, he has been employed in the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is now a Professor. His current research interests are in integrated circuit design and device fabrication. He has been a consultant to Hewlett-Packard, IBM, Exar, and Signetics. He is coauthor of *Analysis and Design of Analog Integrated Circuits* (Wiley, 1977), and editor of the book *Integrated Circuit Operational Amplifiers* (IEEE Press, 1978). He is President of the Solid-State Circuits Council of the IEEE and is a former Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.