Εισαγωγή στην Πληροφορική και τον Προγραμματισμό Η/Υ

7ο Μάθημα (Β μέρος)

Υλοποίηση πράξεων στο δυαδικό σύστημα μέσω Λογικών συναρτήσεων
~~Λογικές πύλες, Λογικές Πράξεις. Λογικές συναρτήσεις.~~
~~Λογικά Κυκλώματα & Άλγεβρα Μπουλ~~

Λεωνίδας Αλεξόπουλος

Αν. Καθηγητής ΕΜΠ

E-mail: leo@mail.ntua.gr

Τηλ: 210 772-1666

Σύνοψη Μέχρι Σήμερα:

Στα προηγούμενα μαθήματα μάθαμε το **Δυαδικό Σύστημα**

→ Κωδικοποίηση – Επεξεργασία – Αποκωδικοποίηση

→ Bit/Byte/Word

→ Κωδικοποίηση αριθμών

→ Παράσταση Ακέραιων Θετικών / Αρνητικών, Fixed & Floating point, Πρόσθεση, Αφαίρεση, Πολλαπλασιασμός,

→ Κωδικοποίηση άλλων δεδομένων

→ Χαρακτήρες, Εικόνα, Ήχος, Αναλογικό Σήμα

→ Μετατροπή Αναλογικού Σήματος σε Ψηφιακό (ADC/DAC), Μέθοδοι Επαλήθευσης Δεδομένων

Πως η θεωρία αυτή υλοποιείται σε επίπεδο Η/Υ?

Transistor

Λογικά Κυκλώματα, Λογικών συναρτήσεις, Λογικές πύλες, Λογικές Πράξεις

Σήμερα:

Μέρος 1ο: (όχι στο Forouzan – εκτός ύλης)

Εισαγωγή σε

- Transistors
- Υλοποίηση με Transistor
- Κατασκευή Transistors (εκτός ύλης)

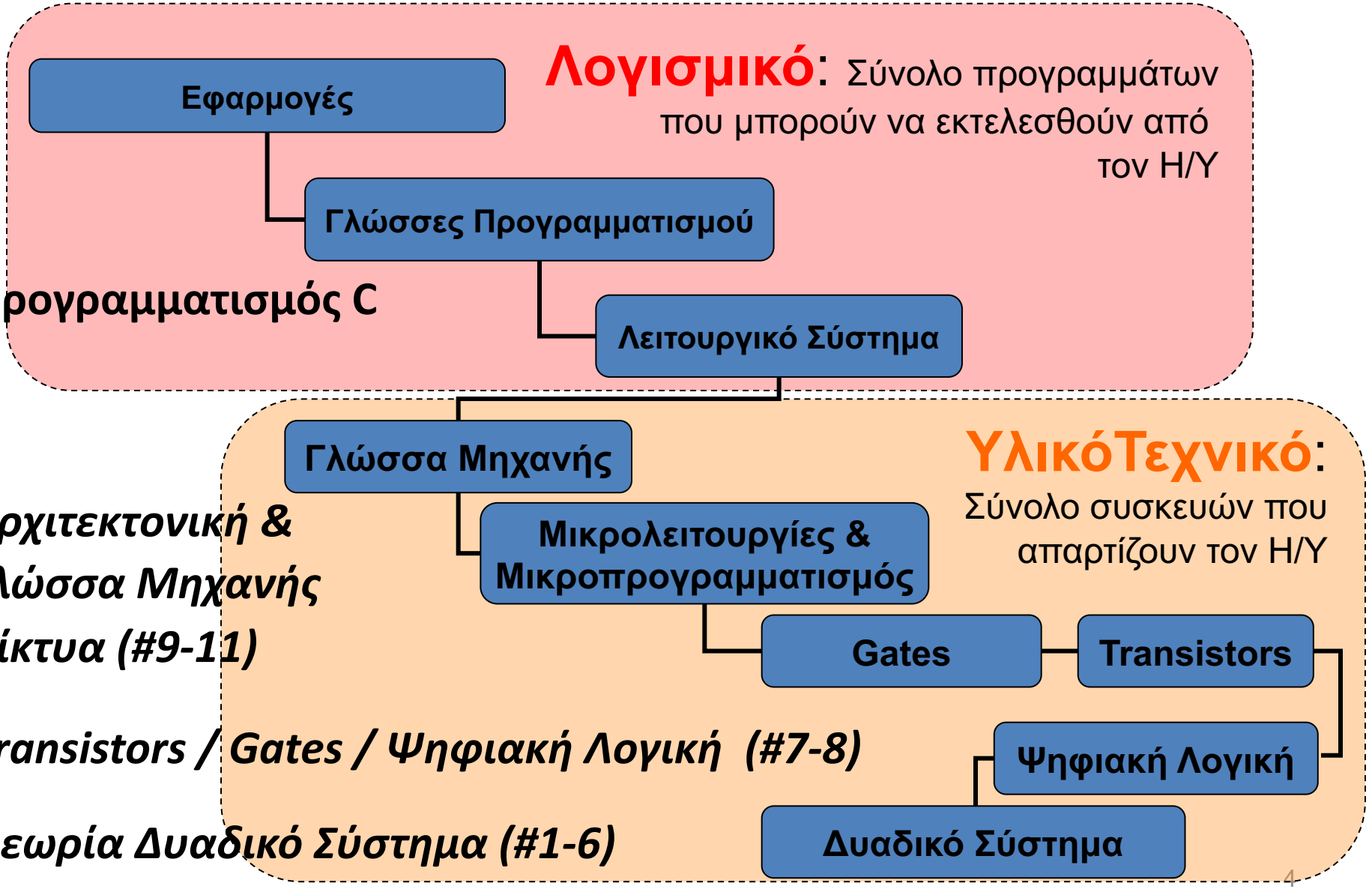
~~**Μέρος 2ο:**~~

~~Forouzan: μόνο 4.1 & Παράρτημα Ε (εκτός 4.2/4.3)~~

~~**Εισαγωγή σε:**~~

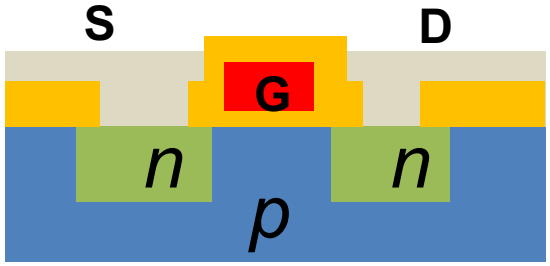
- ~~Λογικές μεταβλητές, πύλες, συναρτήσεις~~
- ~~Πίνακας αληθείας, Σύνθεση/ Ανάλυση~~
- ~~Παραδείγματα / Ασκήσεις~~

Εισαγωγή στην Πληροφορική και τον Προγραμματισμό Η/Υ:



Transistor

Ελέγχουν την διέλευση ρεύματος από S → D



Polysilicon

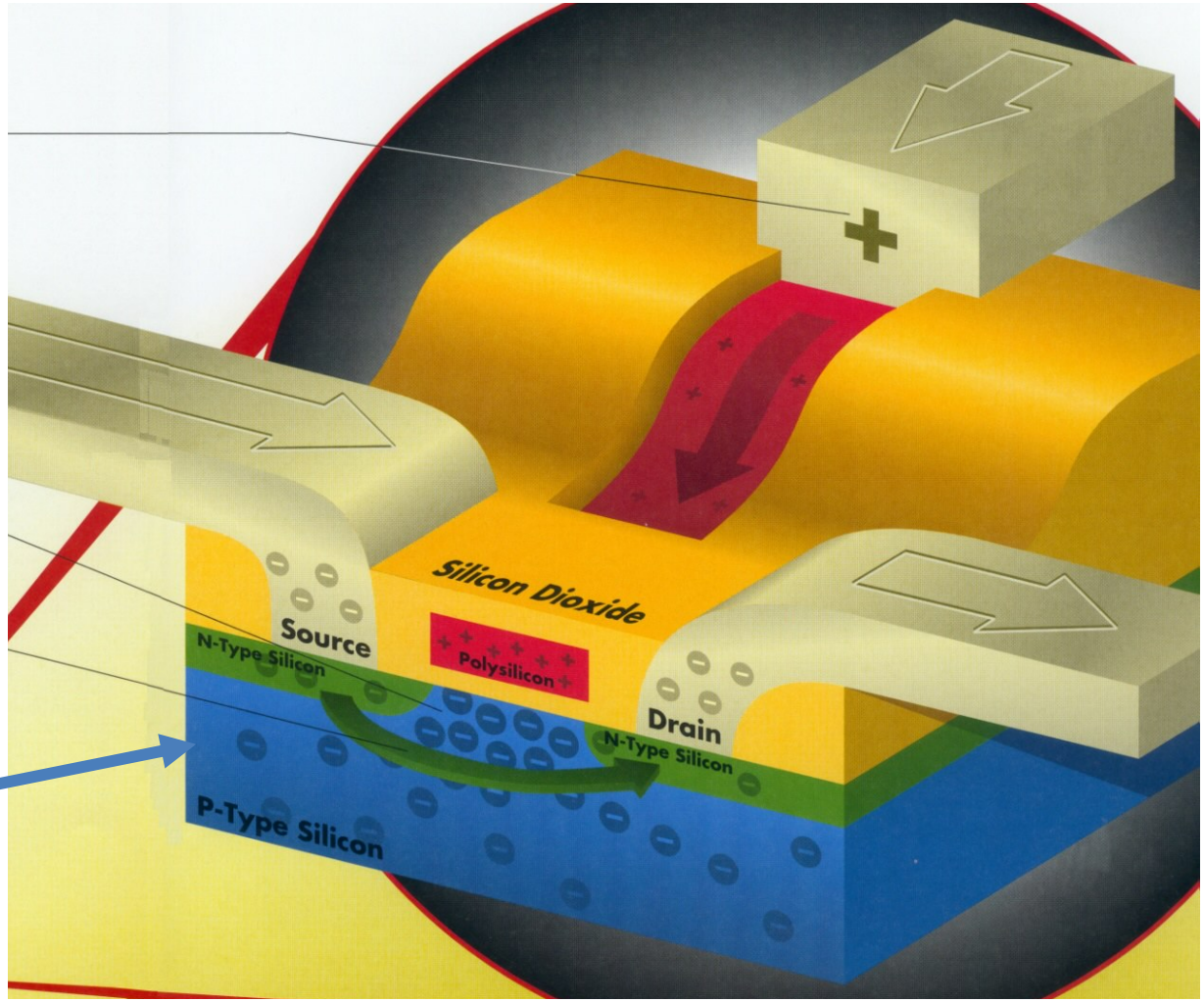
Metal

p substrate

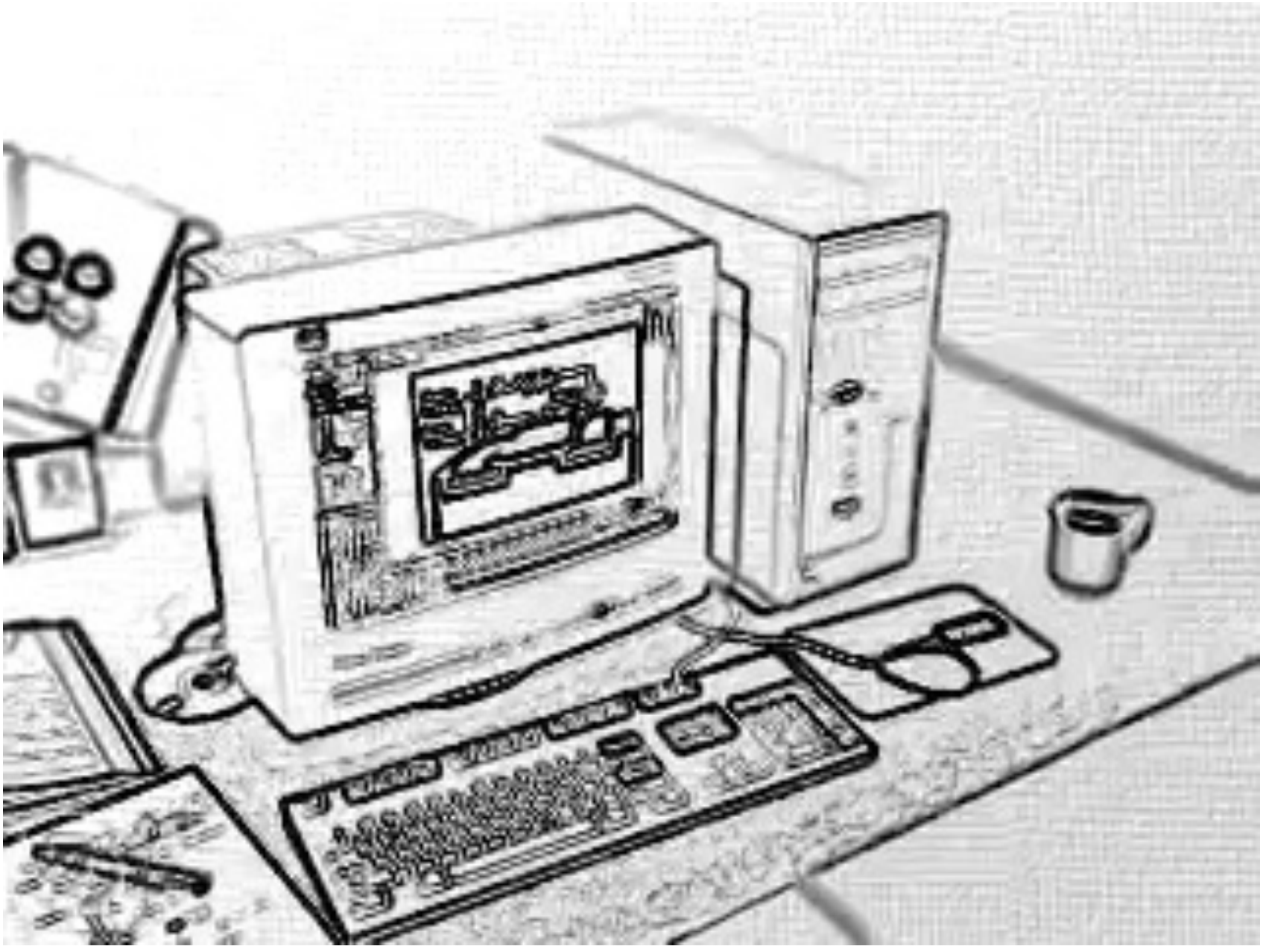
n material

SiO2

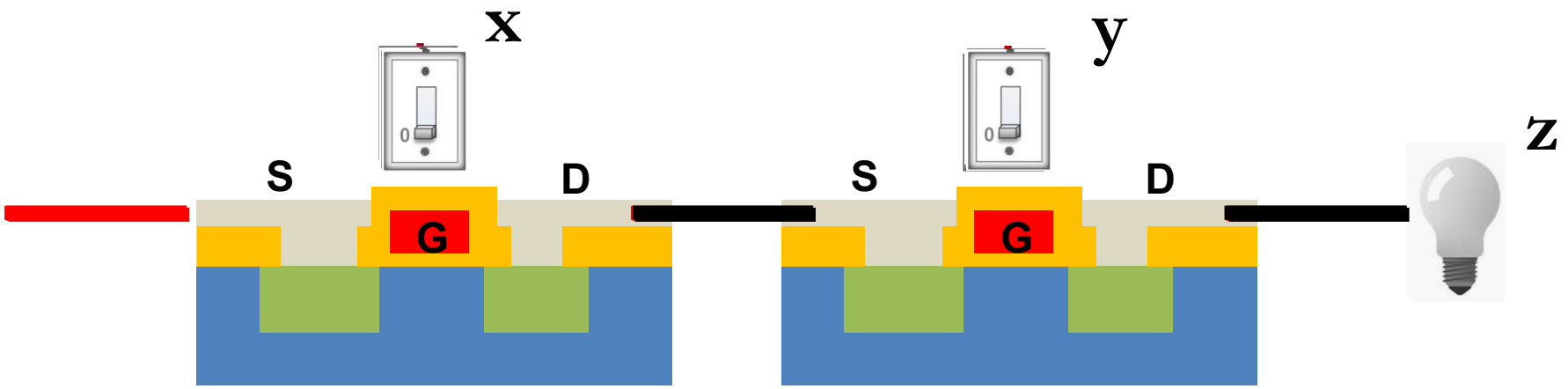
Silicon (πυρίτιο)

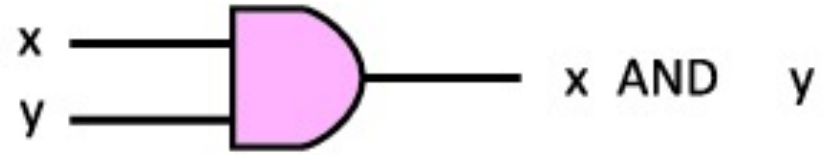


Transistors σε Η/Υς



Πράξεις με transistors

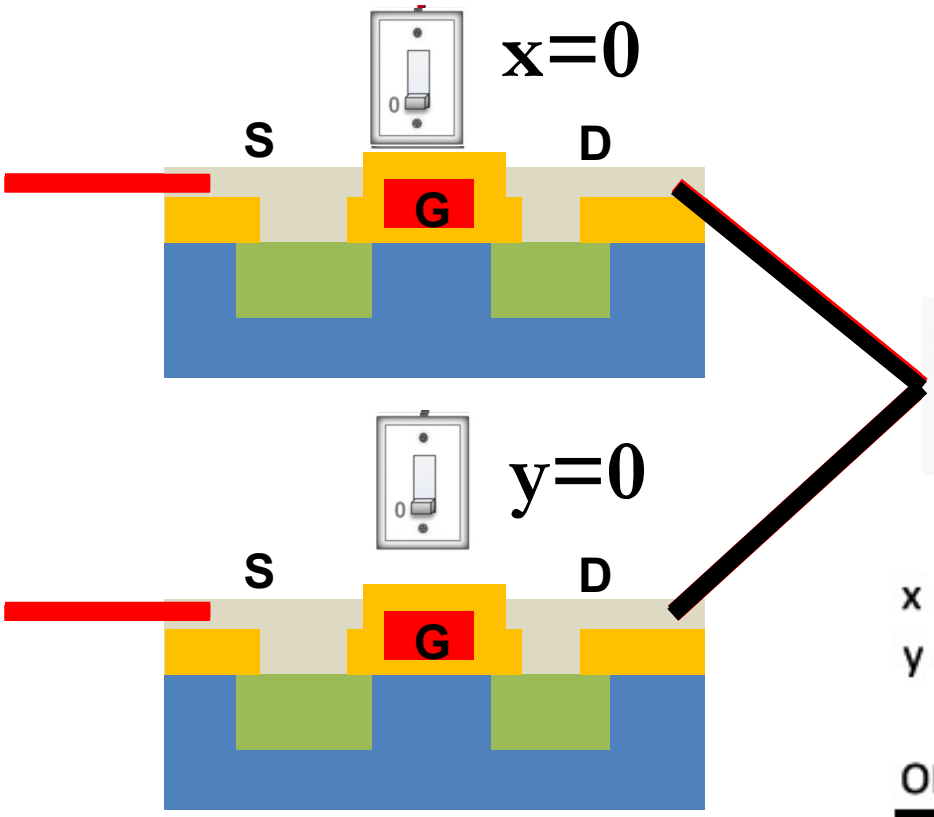




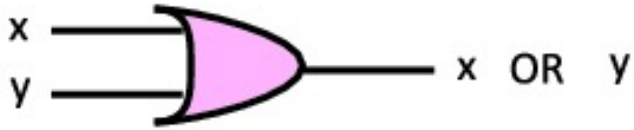
AND

x	y	x AND y
0	0	0
0	1	0
1	0	0
1	1	1

Πράξεις με transistors



z=0

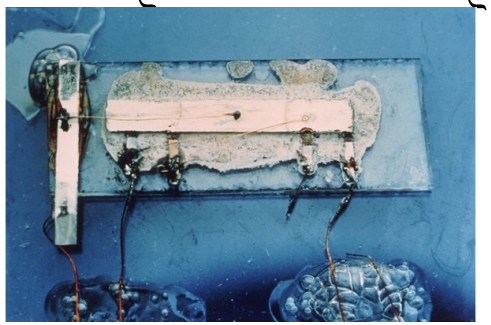


OR

x	y	x OR y
0	0	0
0	1	1
1	0	1
1	1	1

Ηλεκτρονική Υλοποίηση Πυλών

- Αν συνδυάσουμε, κατάλληλα ολοκληρωμένα, μεγάλο αριθμό τρανζίστορ μπορούμε να υλοποιήσουμε περισσότερες πύλες από αυτές που αντιστοιχούν στον ίδιο αριθμό τρανζίστορ μεμονωμένα. Ανάλογα με τον αριθμό των τρανζίστορ που χρησιμοποιούμε προκύπτουν οι παρακάτω περιπτώσεις:



1950

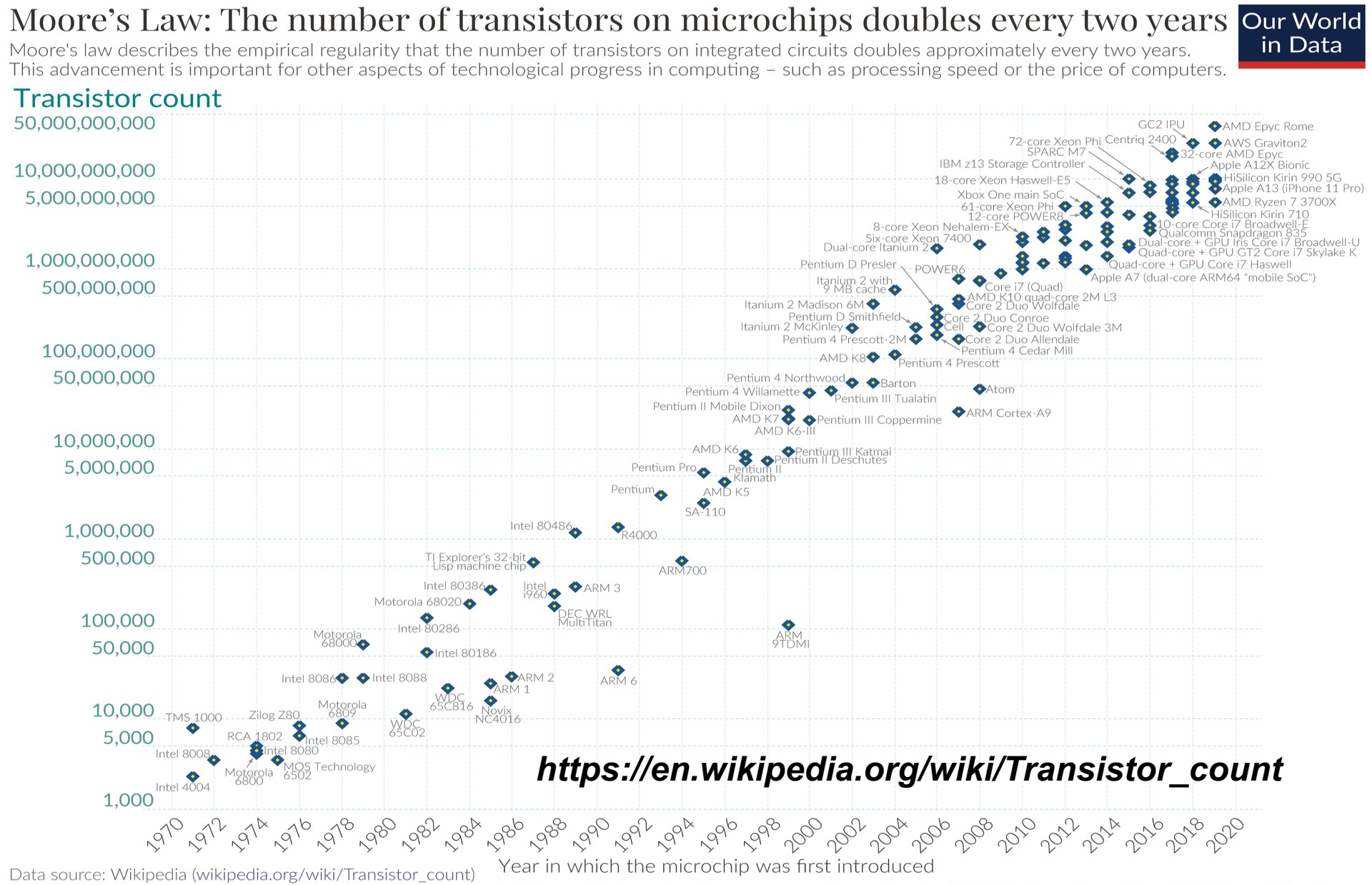
2000 (VLSI)

Αρ.		
	SSI	Small Scale Integration (1960)
~100	**MSI**	Medium Scale Integration
~1000	**LSI**	Large Scale Integration
~10^6	**VLSI**	Very Large Scale Integration (1970)
~10^9	**ULSI**	Ultra Large Scale Integration

2021 up to trillions….

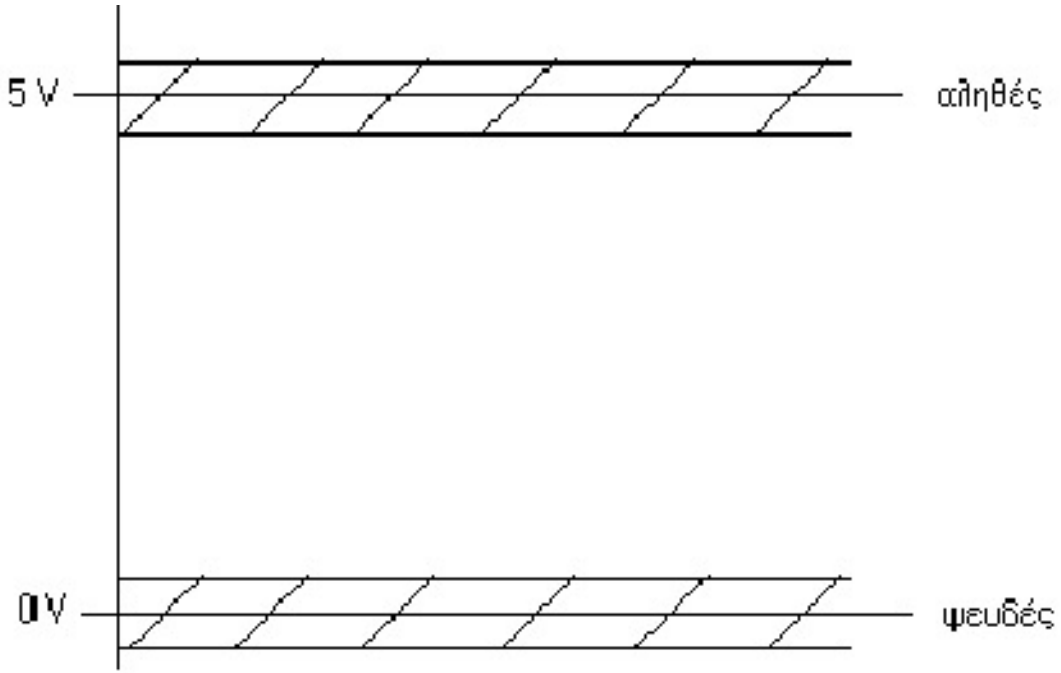
- Τα VLSI/ULSI είναι μικρά, παρουσιάζουν μικρή κατανάλωση ηλεκτρικής ενέργειας (άρα εκλύουν λιγότερη θερμότητα), είναι αξιόπιστα και το κόστος παραγωγής τους συνεχώς ελαττώνεται.

Αριθμός transistors per circuit chip



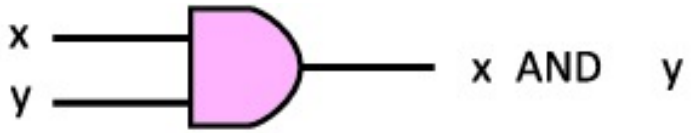
Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

Αληθές (1) / Ψευδές (0) → 0 / +5 Volt

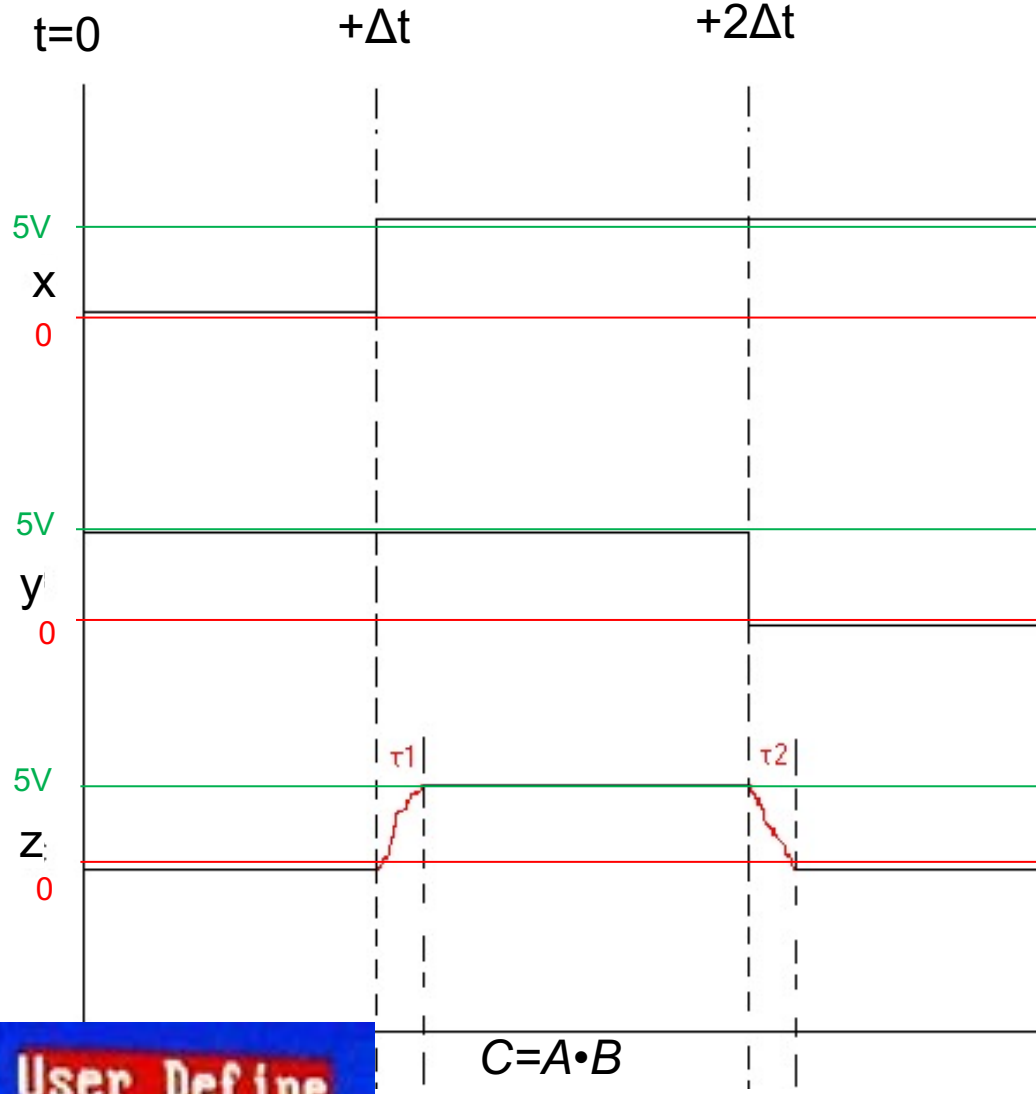


- Κατά την ηλεκτρονική υλοποίηση τύπου TTL (Transistor – to – Transistor Logic) αντιστοιχίζουμε το λογικό “0” (ψευδές) με τάση 0 Volt και το λογικό “1” (αληθές) με τάση +5 Volt. Όμως το αληθές και το ψευδές δεν αντιστοιχούν με απόλυτη ακρίβεια στα +5 και 0 Volt, αλλά σε μια *περιοχή* γύρω από αυτά.

Συχνότητα Υλοποίησης λογικής πράξης

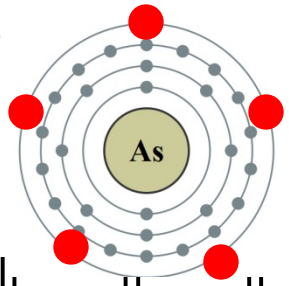


- Έστω η λογική συνάρτηση
  $Z = f(X,Y) = X \bullet Y = X$ *AND* Y
- Παρατηρούμε ότι στις μεταβατικές καταστάσεις βρισκόμαστε εκτός των ορισθέντων ορίων για μικρό χρόνο ***τ***, που λέγεται ***χρονική καθυστέρηση*** και δείχνει το χρόνο που πρέπει να περάσει από την αλλαγή μιας εισόδου για να σιγουρευτούμε για την τιμή της εξόδου.
- **Η περίοδος του συστήματος πρέπει να είναι μεγαλύτερη από την χρονική καθυστέρηση** για να αποφευχθεί το πρόβλημα του να βρεθεί το σύστημα σε «αόριστη» κατάσταση.
- Δηλαδή υπάρχει περιορισμός στη συχνότητα του συστήματος.
- Σήμερα έχει επιτευχθεί δραστική μείωση της χρονικής καθυστέρησης. Έτσι οι σημερινοί υπολογιστές έχουν φτάσει σε συχνότητες, της τάξης των GHz.

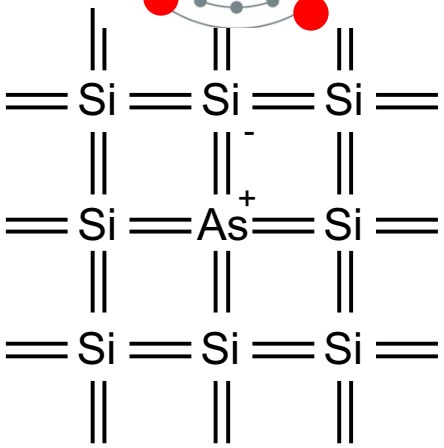


Κατασκευή Transistor

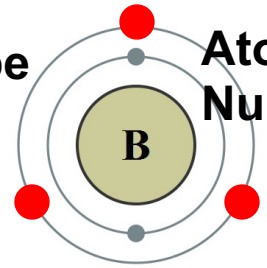
AN: 33

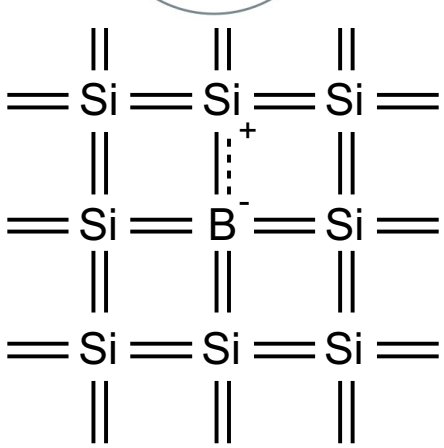


n-type

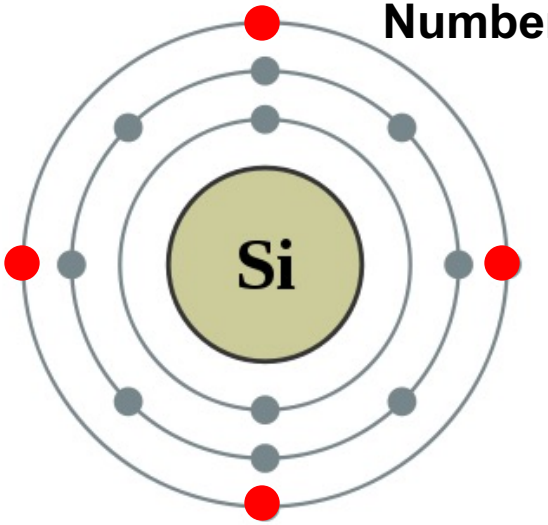


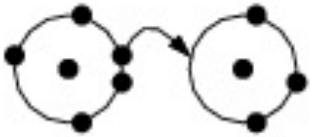
p-type **Atomic Number:** 5



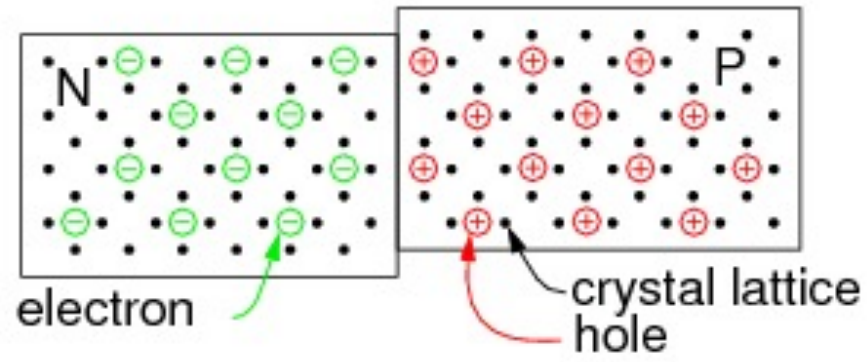


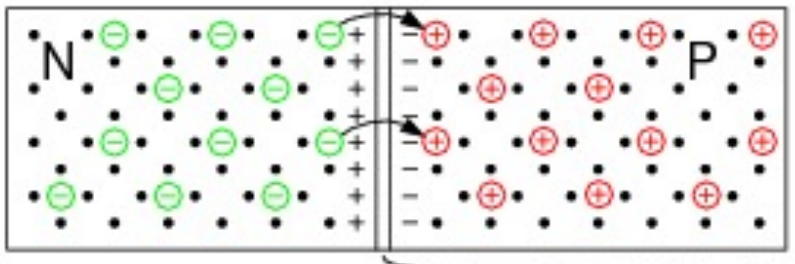
Atomic Number: 14

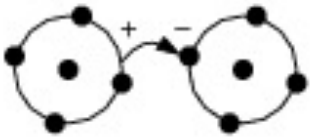




no charge separation



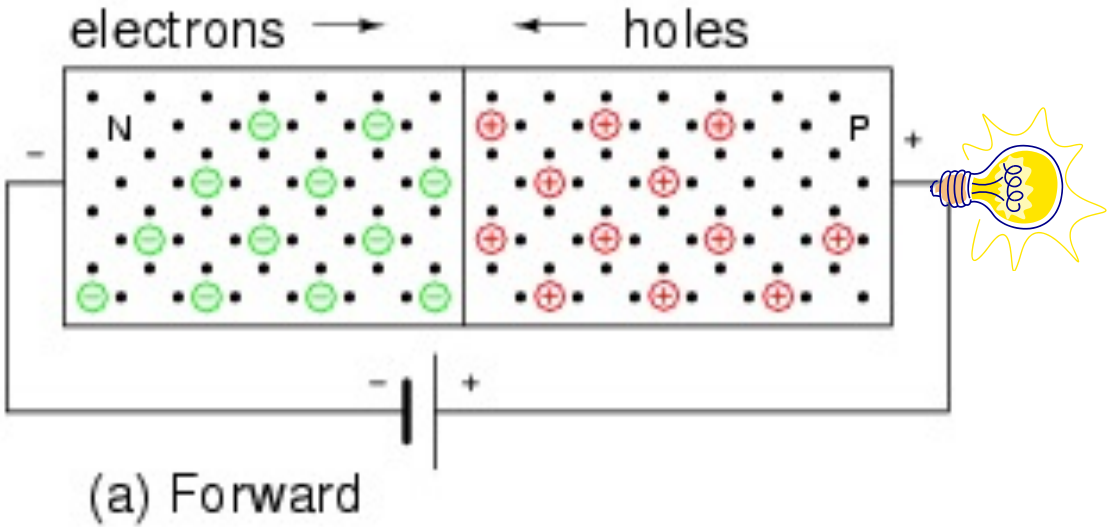




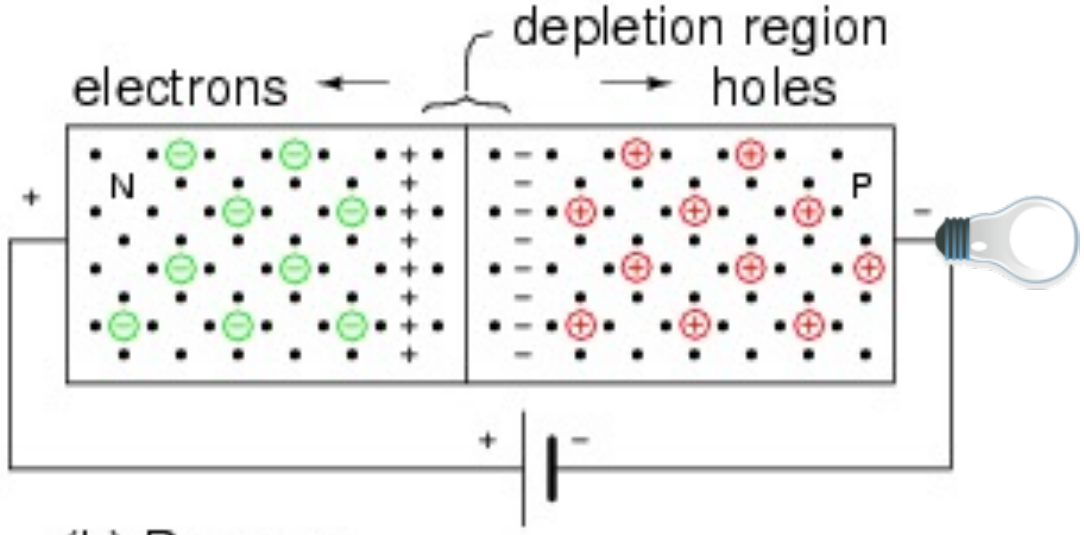
charge separation

http://www.allaboutcircuits.com/vol_3/chpt_2/6.html

Κατασκευή Transistor



(a) Forward



(b) Reverse

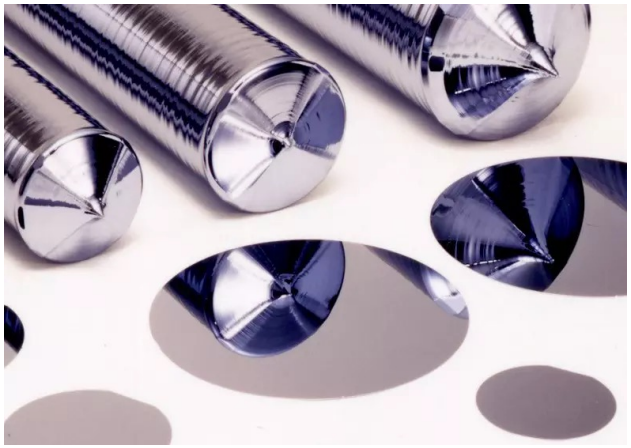
Κατασκευή Transistor

Clean Rooms

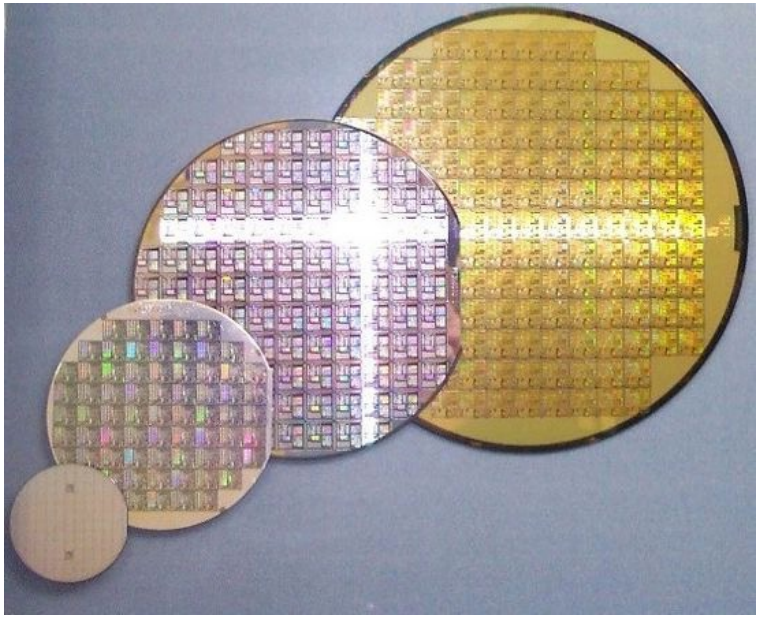
Κατασκευή Transistor

1. Sand (Si)

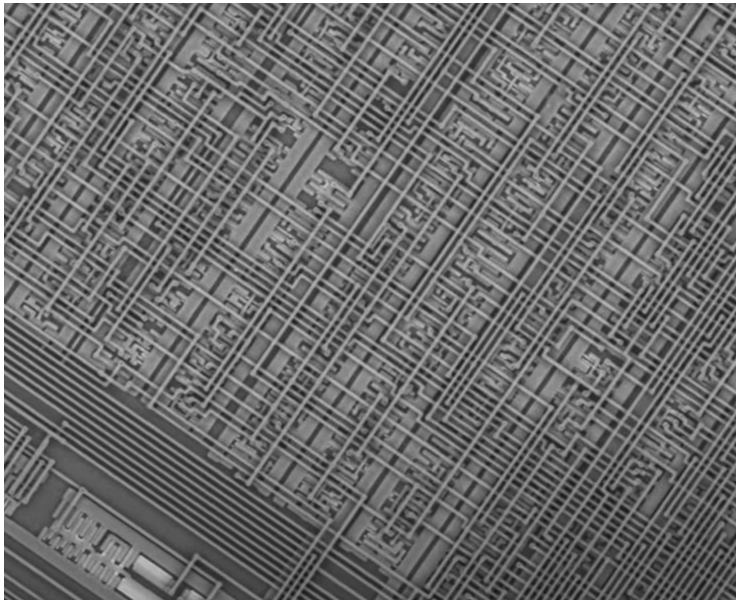
2. Wafers 2/4/6/8/12 inches



3. Photolithography on wafers



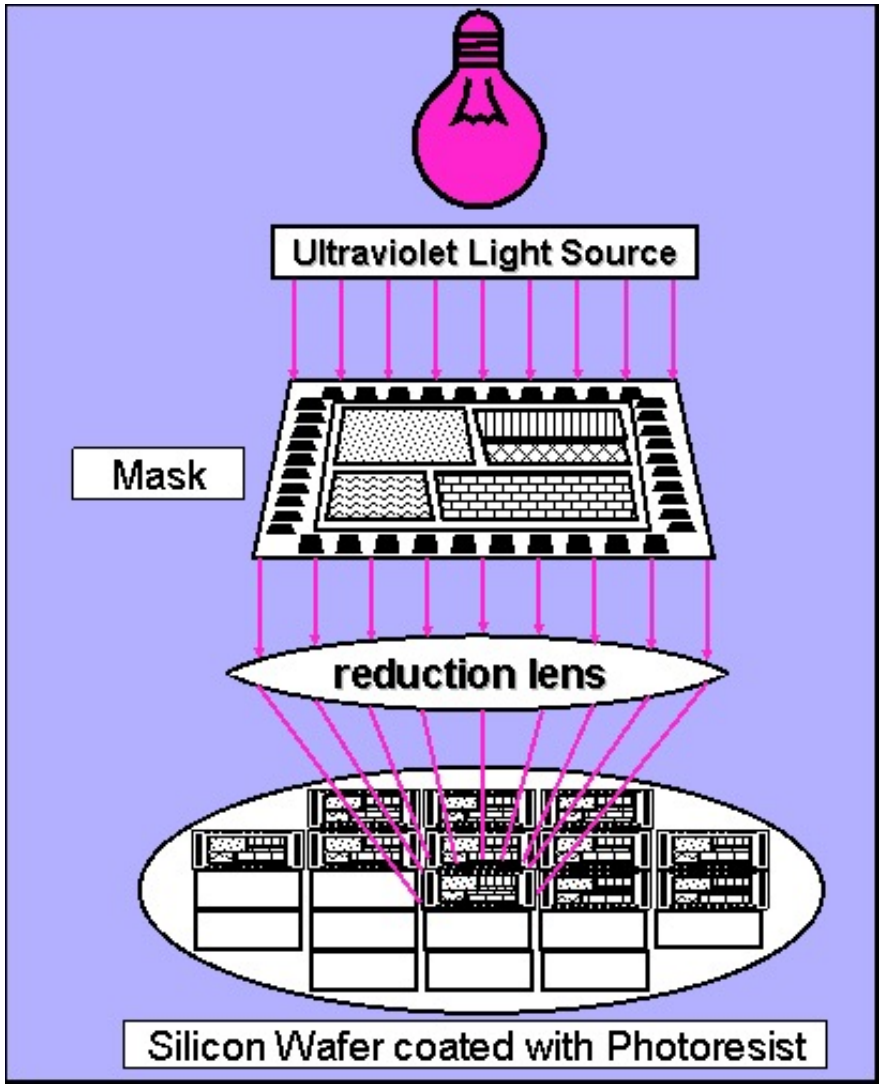
4. Wafers with several layers



Photolithography on wafers

https://pt.coursera.org/lecture/nanotechnology/photolithography-sample-patterning-demonstration-TdtAR

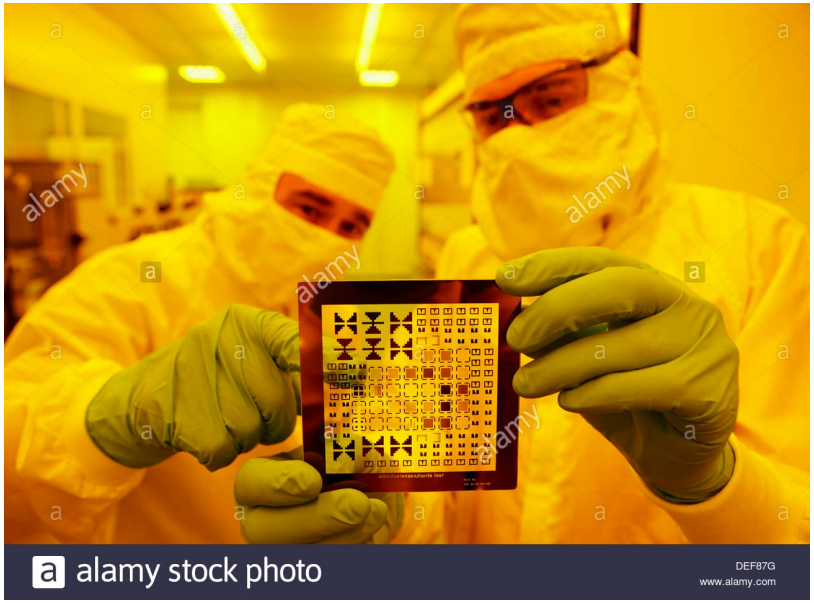
Photolithography



REF: https://billgascoyne.wordpress.com/eda-in-a-nutshell/

Wafer

Mask



Photolithography on wafers

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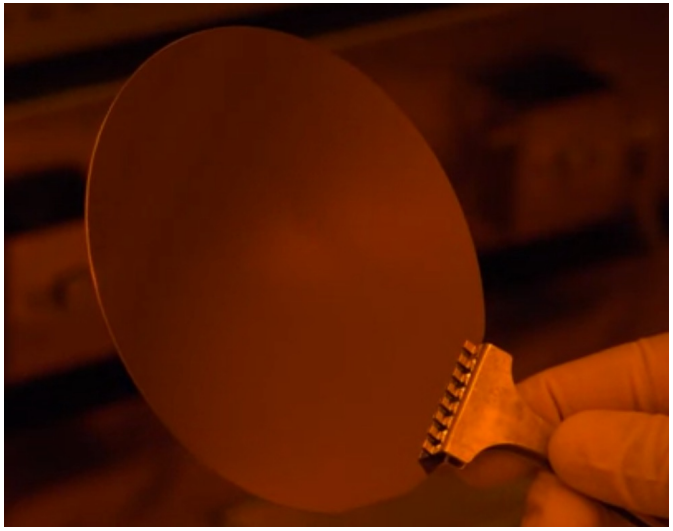
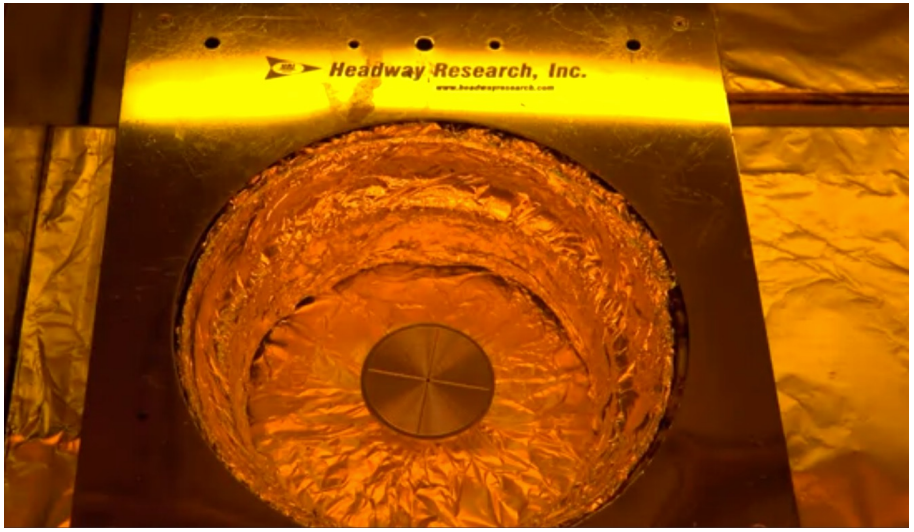
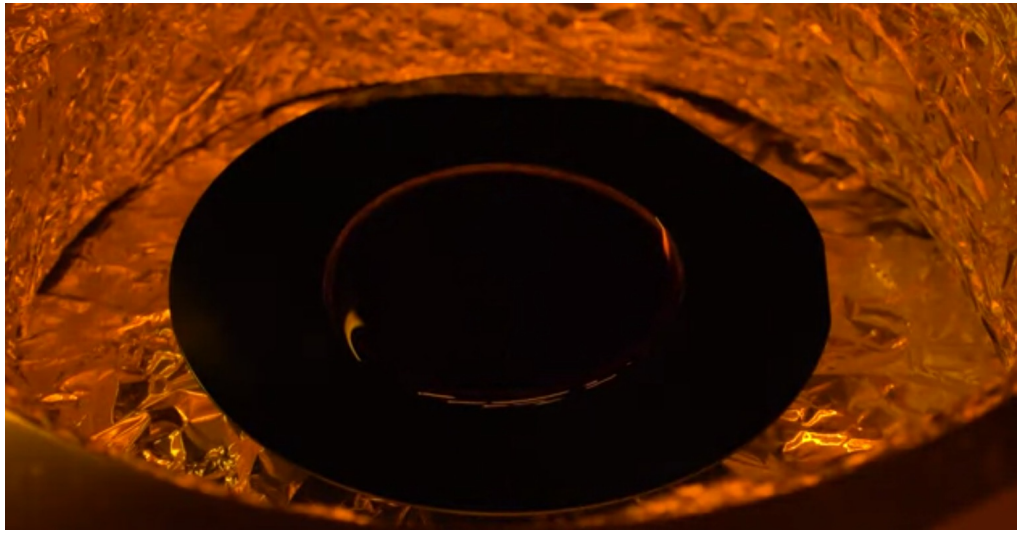
Wafer



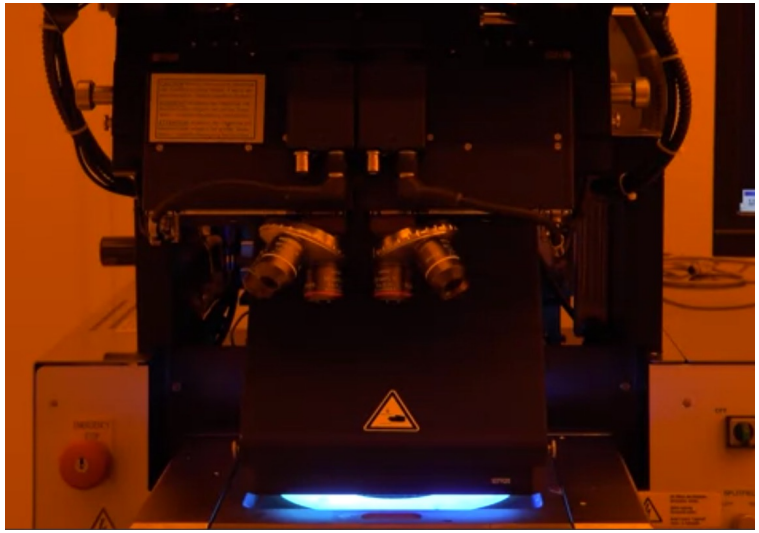
Spin Coater



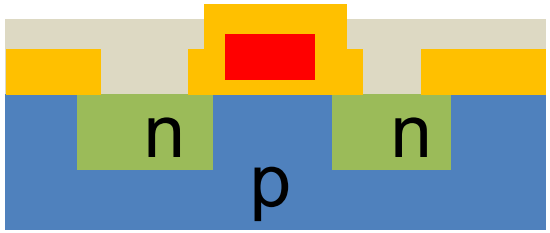
Photoresist



Exposure



Κατασκευή Transistor



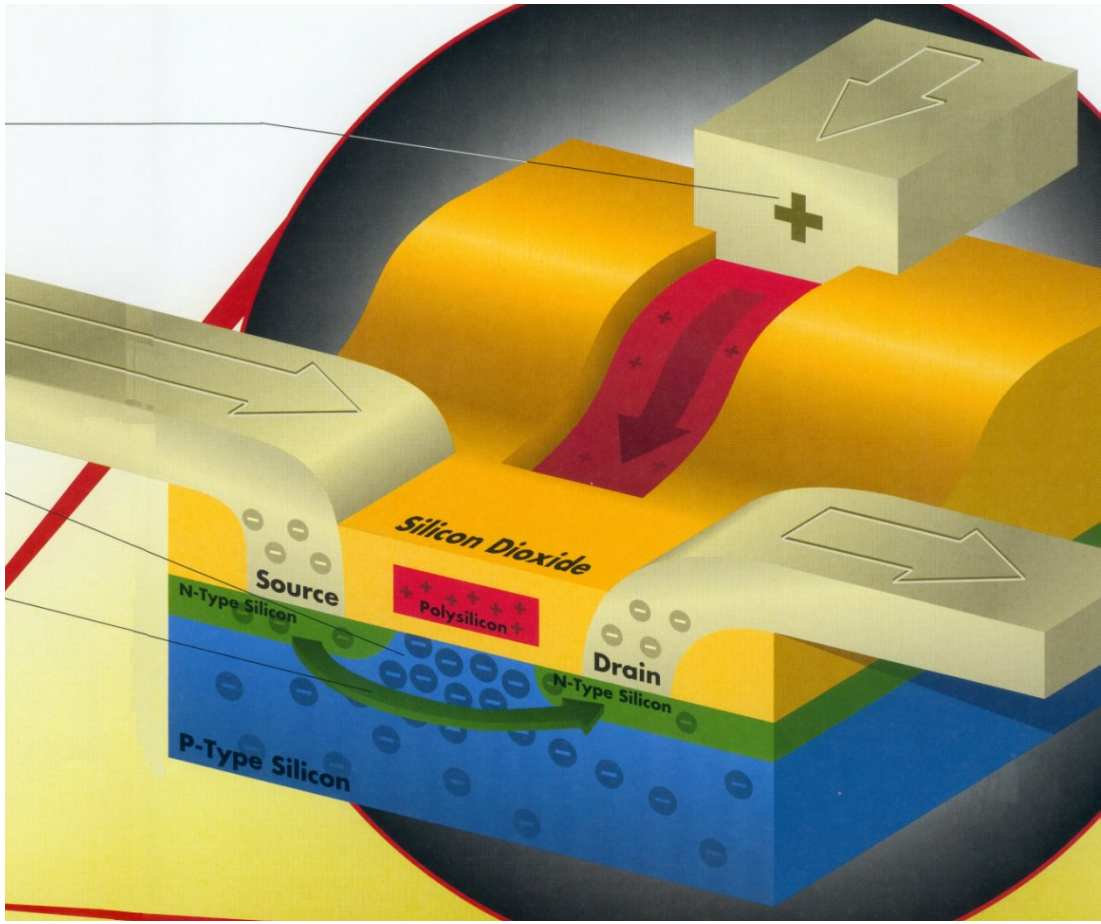
Polysilicon

Metal

p substrate

n material

SiO2

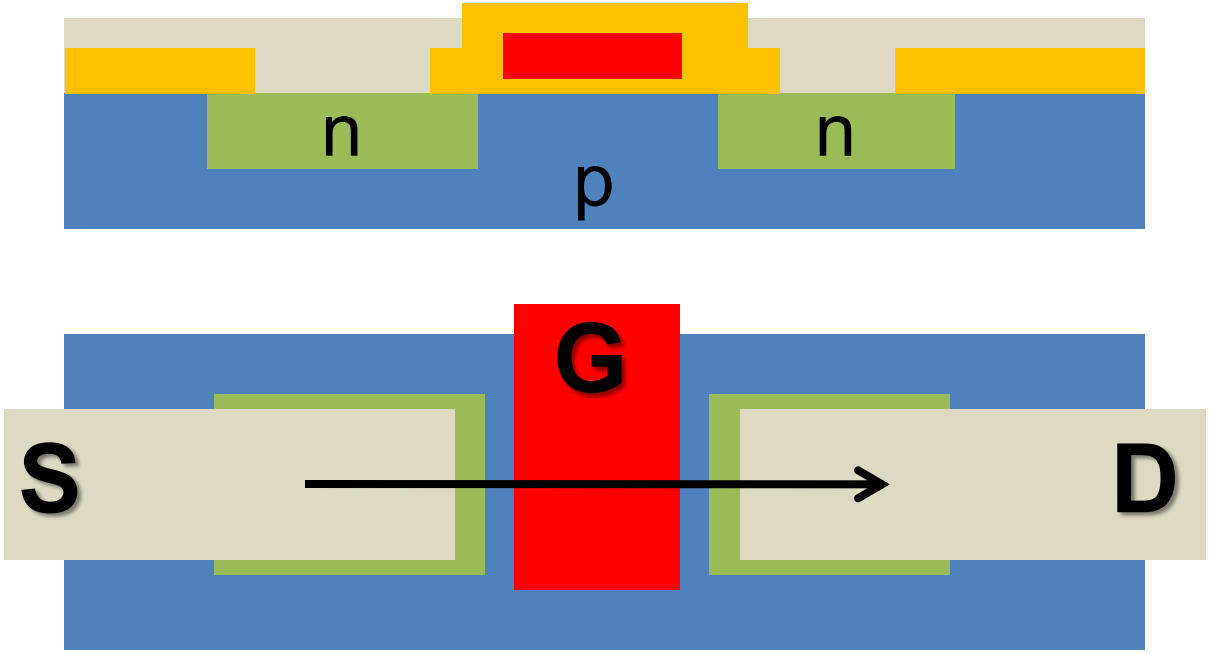


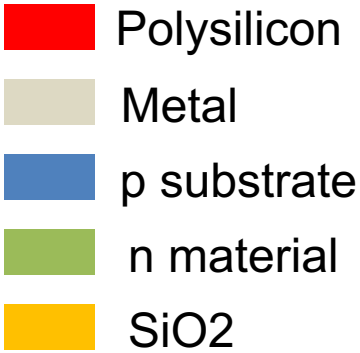
www.cmosvlsi.com/lect0.ppt

http://lsmwww.epfl.ch/Education/former/2002-2003/VLSIDesign/ch02/ch02.html

http://www2.renesas.com/fab/en/line/line1.html

Transistor Cross-section





→ Cover wafer with protective layer of SiO_2 (oxide)
→ Spin photoresist
→ n-well mask
→ Etch oxide with hydrofluoric acid (HF!)
→ Strip off remaining photoresist (Piranah!)
→ Place wafer in furnace and heat until As atoms diffuse into exposed Si
→ Strip off the remaining oxide using HF
→ Deposit very thin layer of gate oxide
→ Place wafer in furnace with Silane gas (SiH_4) to form polysilicon
→ Polysilicon mask, etch oxide with HF
→ Cover wafer with SiO_2
→ Etch with HF to expose contacts
→ Sputter on aluminum over whole wafer and pattern to remove excess metal, leaving wires

→ **Cover wafer with protective layer of SiO_2 (oxide)**
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Grow SiO_2 on top of Si wafer
900 – 200 C with O_2 in oxidation furnace

→ Cover wafer with protective layer of SiO_2 (oxide)
→ **Spin photoresist**
→ n-well mask
→ Etch oxide with hydrofluoric acid (HF!)
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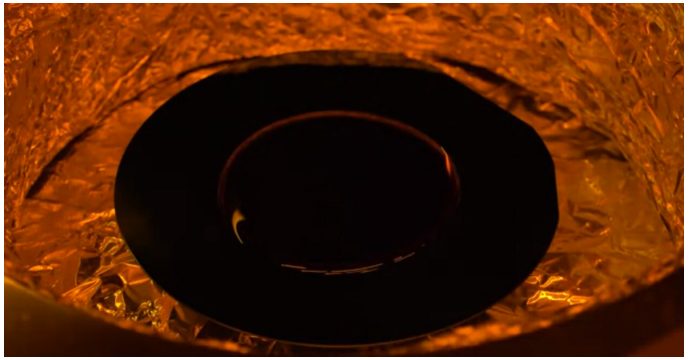

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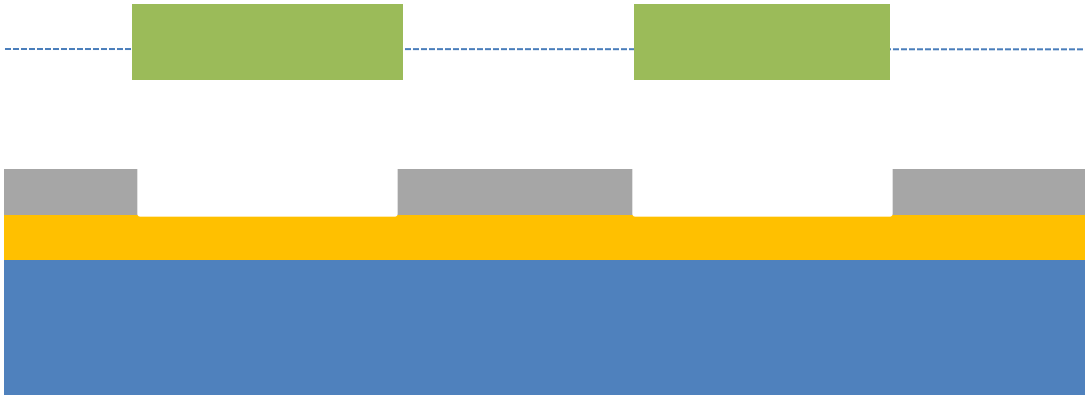
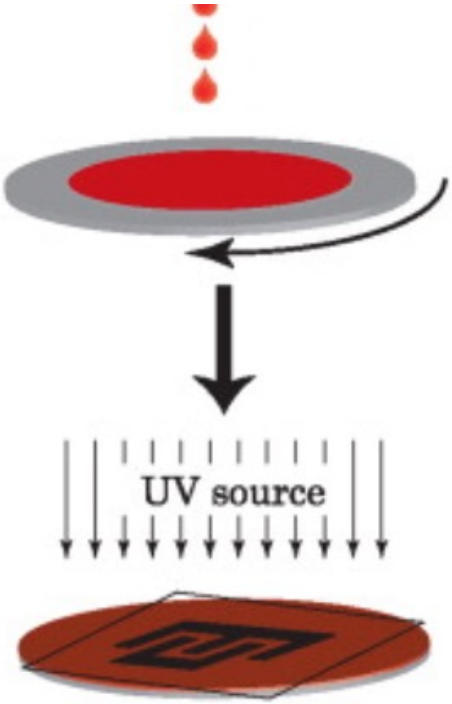
→ .
→.
→.





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→ Strip off remaining photoresist (Piranah!)
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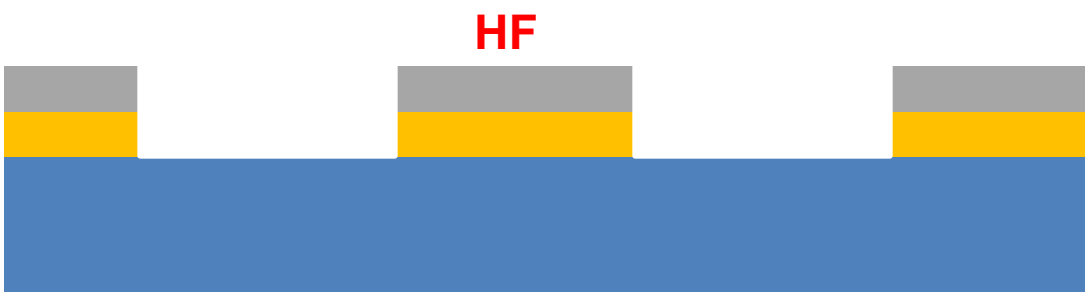
→ Sputter on aluminum over whole wafer and pattern to remove excess metal, leaving wires



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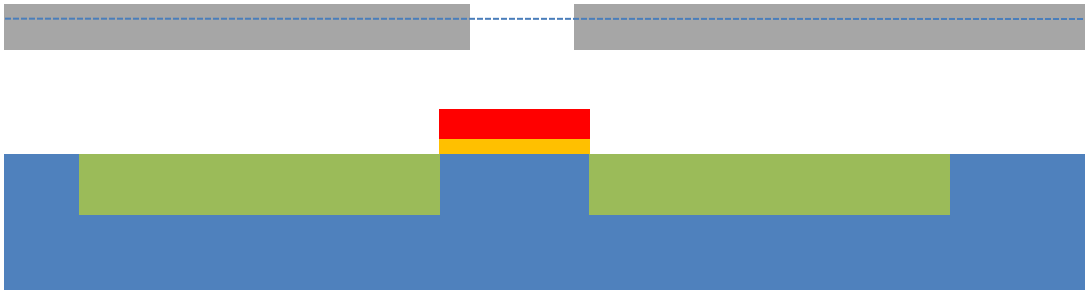

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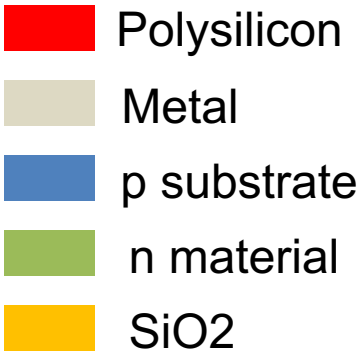

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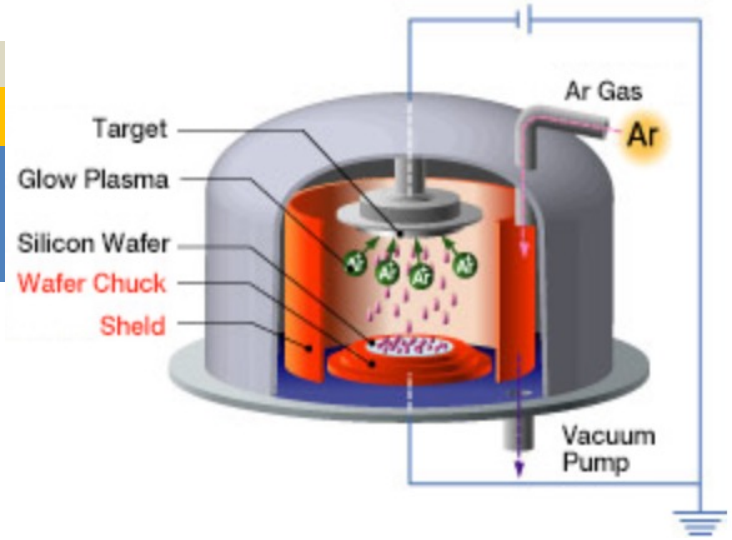
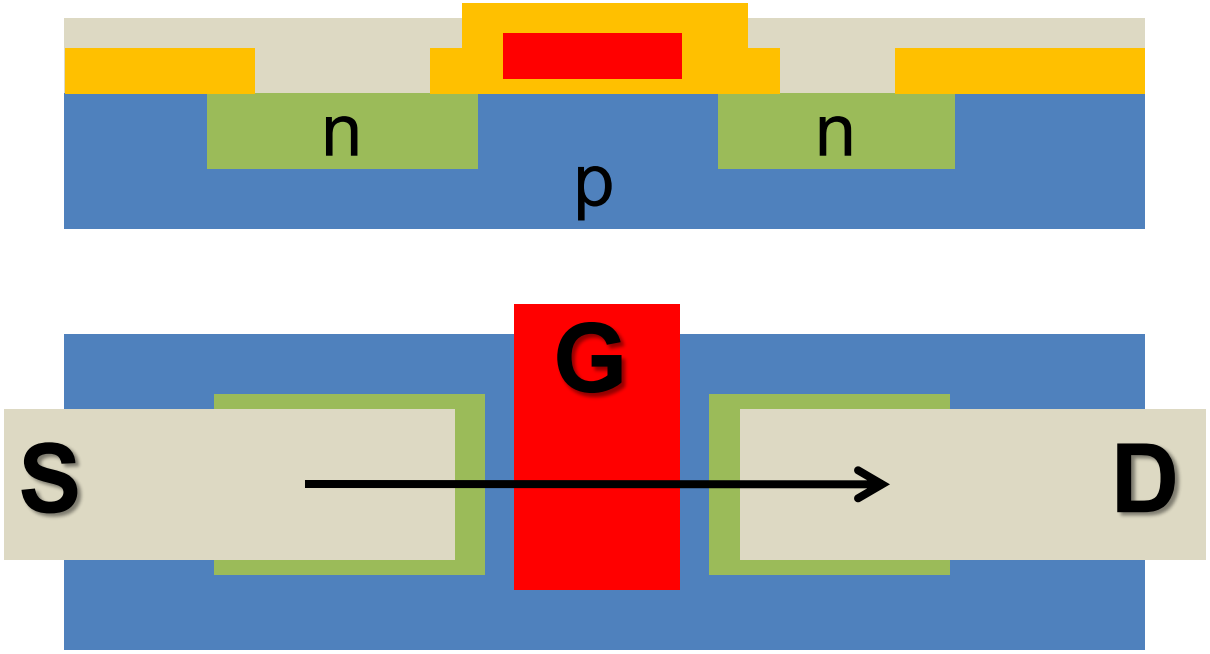
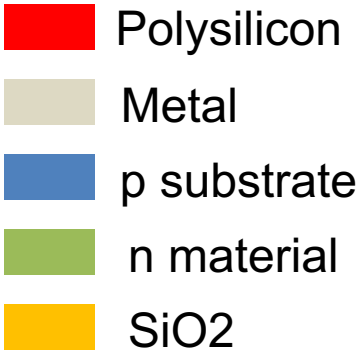
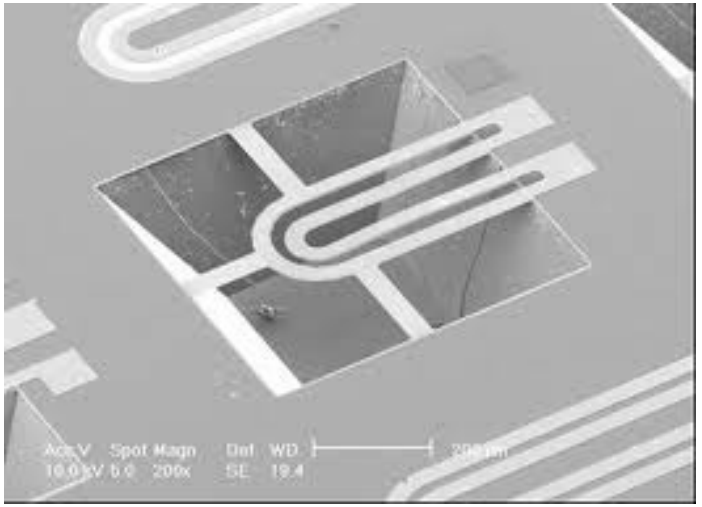


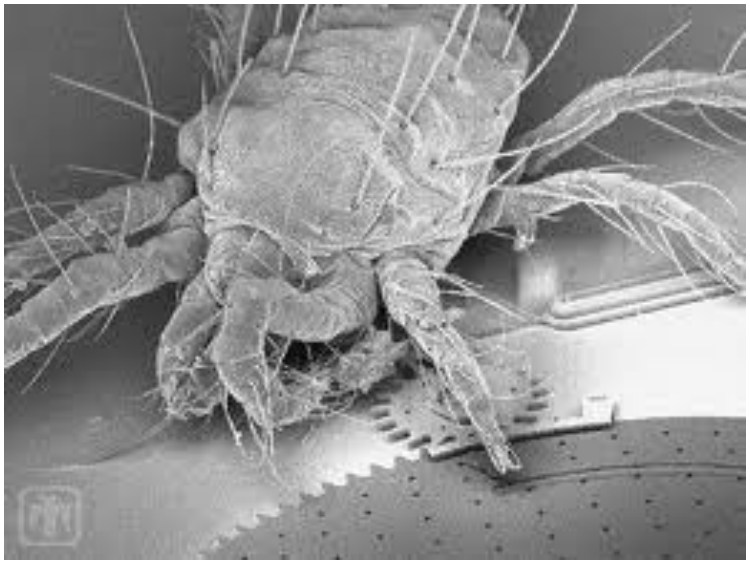
Transistor Cross-section

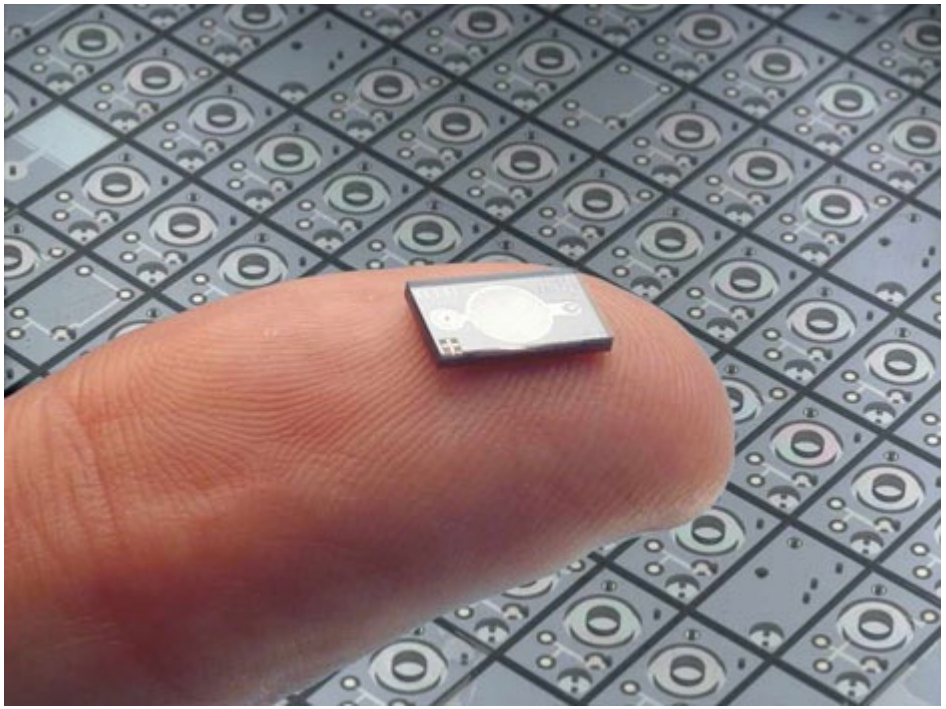




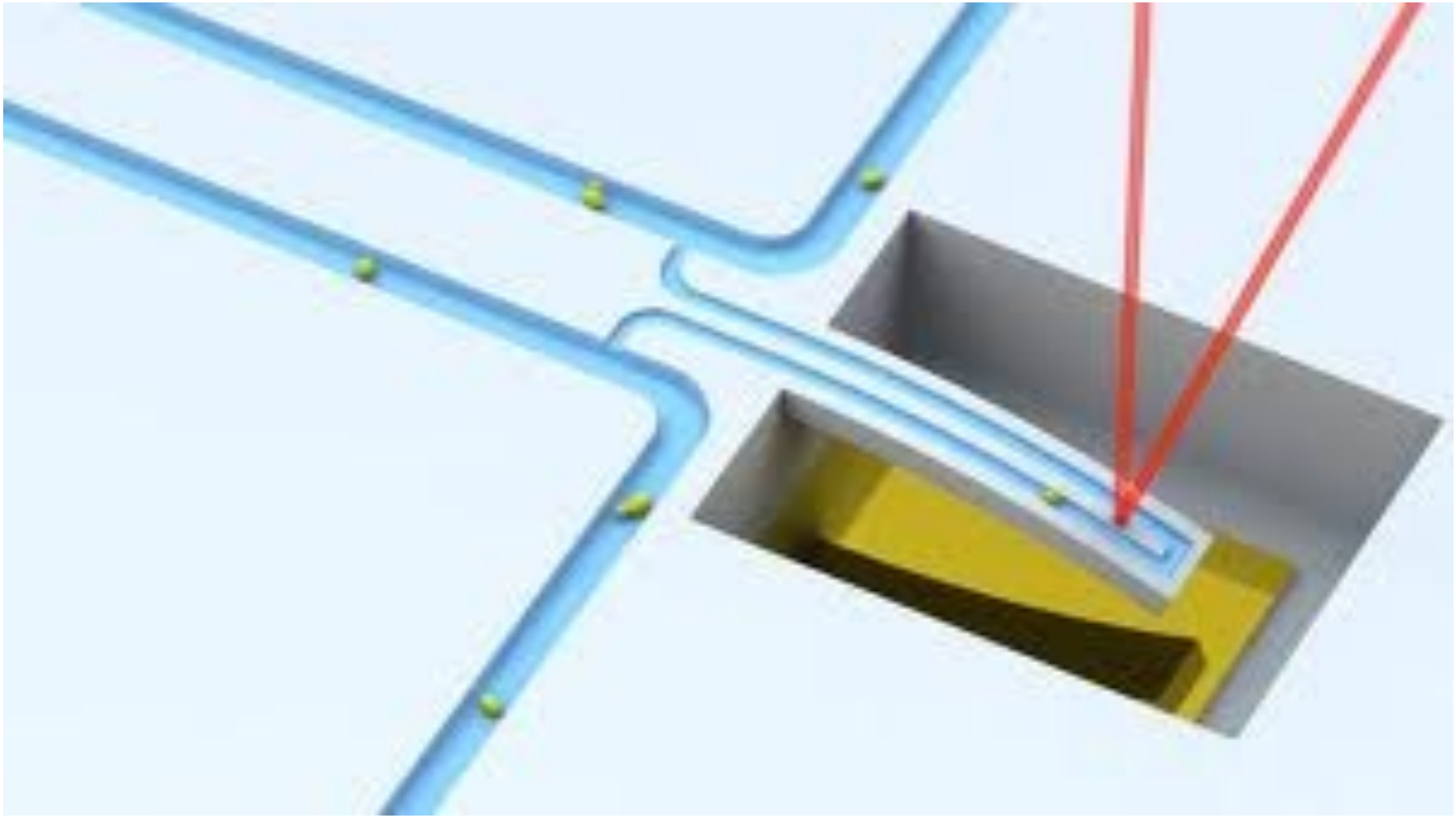
Fab for MEMS





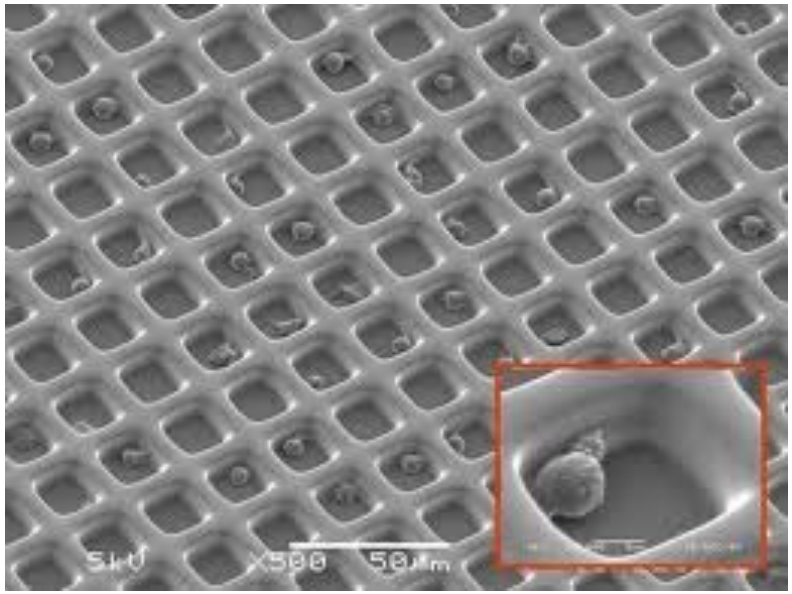


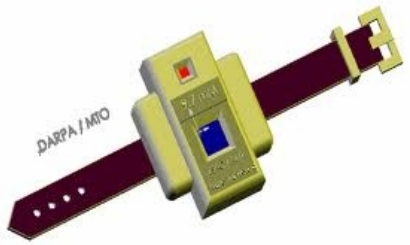
Fab for BIO-MEMS

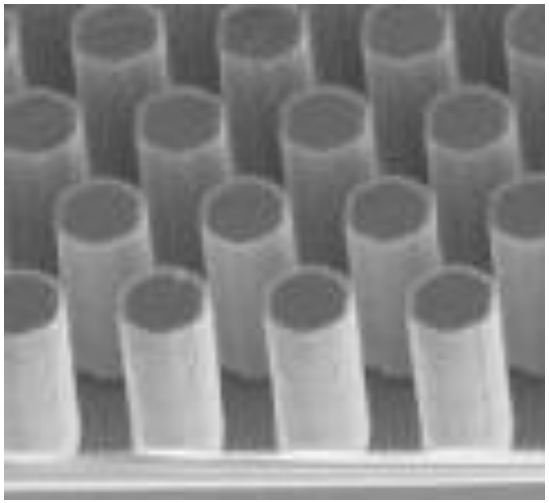


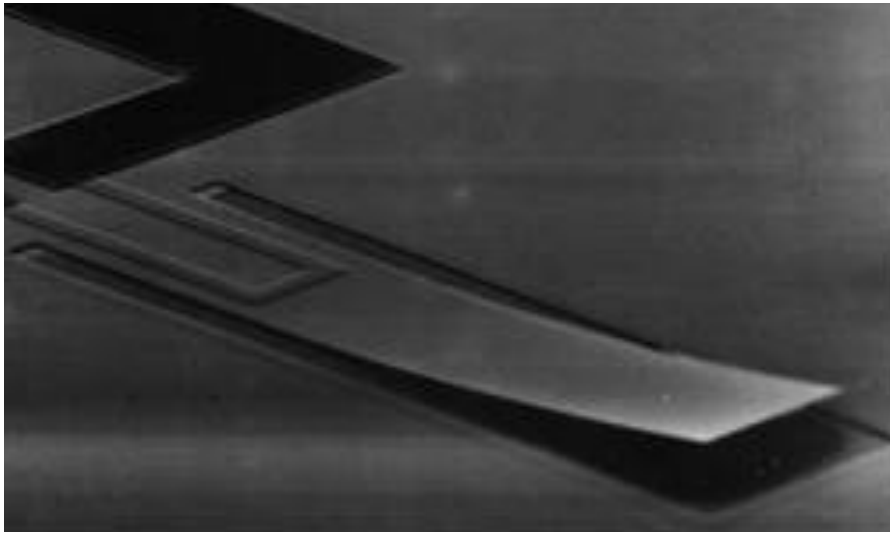
Manalis Lab, MIT

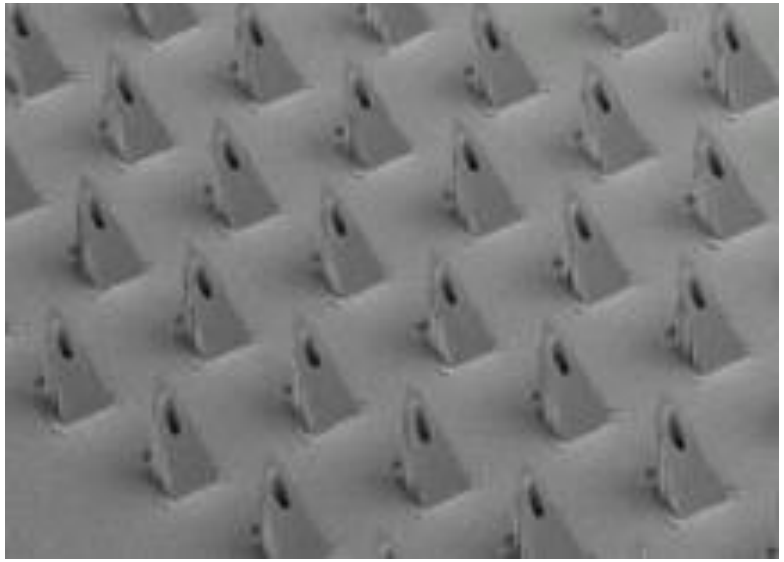
Fab for BIO-MEMS







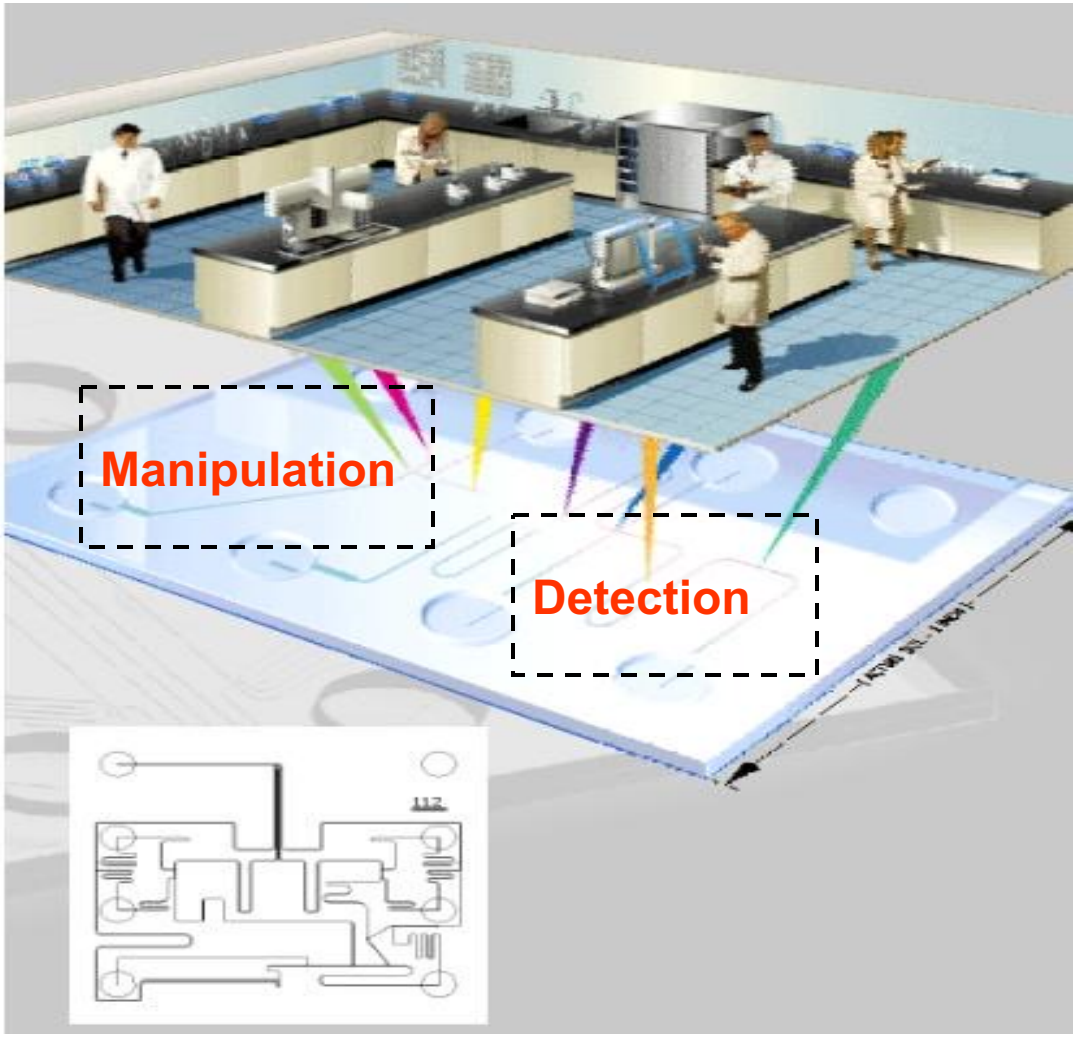




Lab-on-Chip Technology

Features/Benefits

- Miniaturization
- Automation
- Integration
- Data Quality
- Reagent Savings
- Portability
- Precision



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